

Compal Confidential

Tanglha Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M

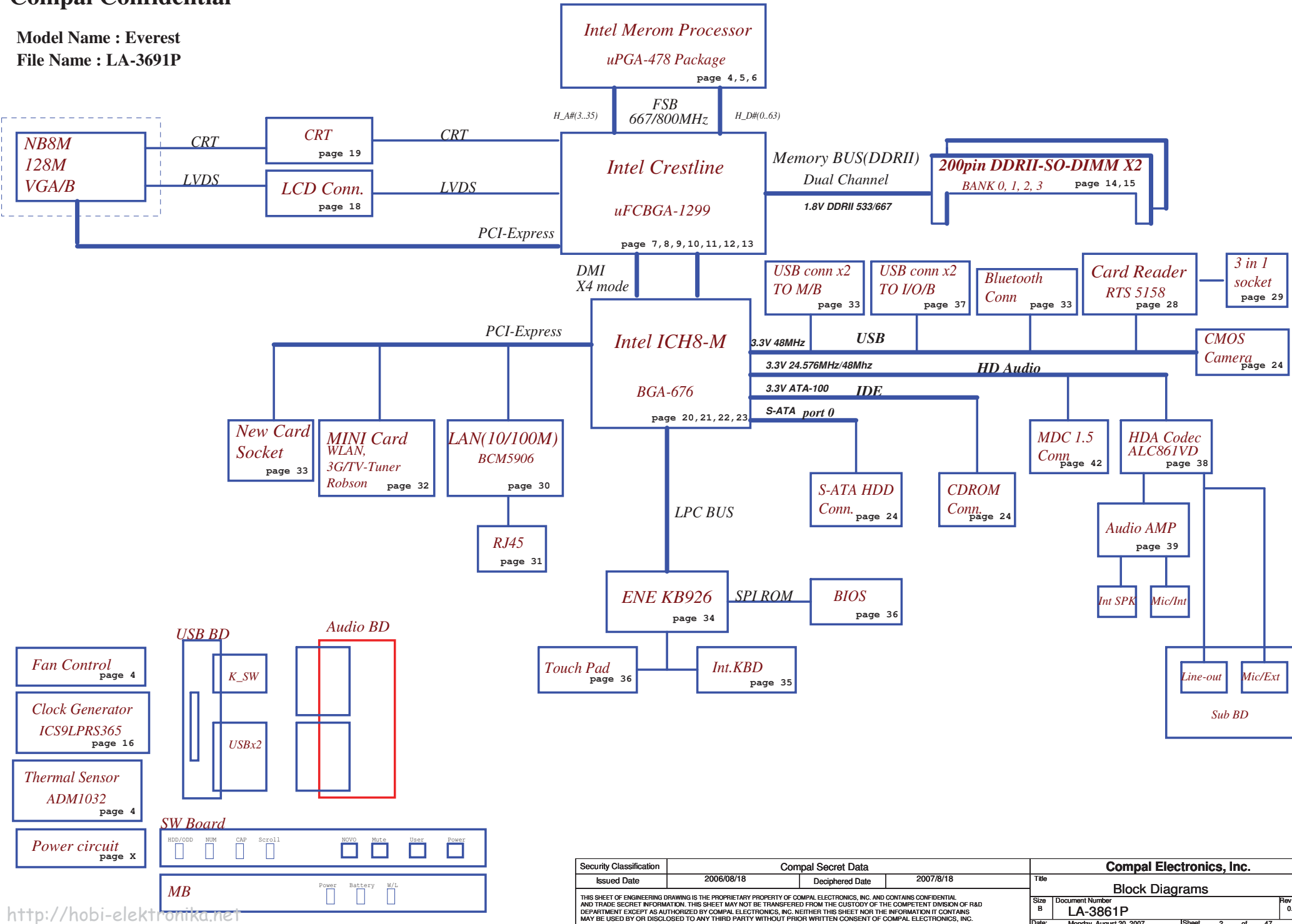
2007-08-16

REV: 1.0

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				Size B	Document Number LA-3861P
Date: Monday, September 03, 2007				Sheet 1	Rev 0.1
				of 47	

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Model Name : Everest
File Name : LA-3691P



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				LA-3861P	Rev 0.1
				Date: Monday, August 20, 2007	Sheet 2 of 47

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0 (R744)	0 (R745)	A-TEST
0 (R744)	1 (R742)	B-TEST
1 (R741)	0 (R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

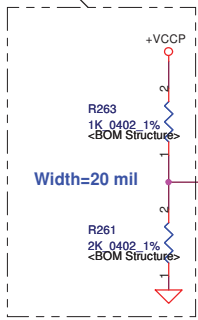
EC SM Bus2 address

Device	Address
GMT-781	1001 100X b
NVIDIA NB8X	

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

Close to CPU pin AD26
within 500mils.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any other
toggling signal.
COMP[0,2] trace width is
18 mils. COMP[1,3] trace
width is 4 mils.

Length match within 25 mils.
The trace width/space/other is
20/7/25.

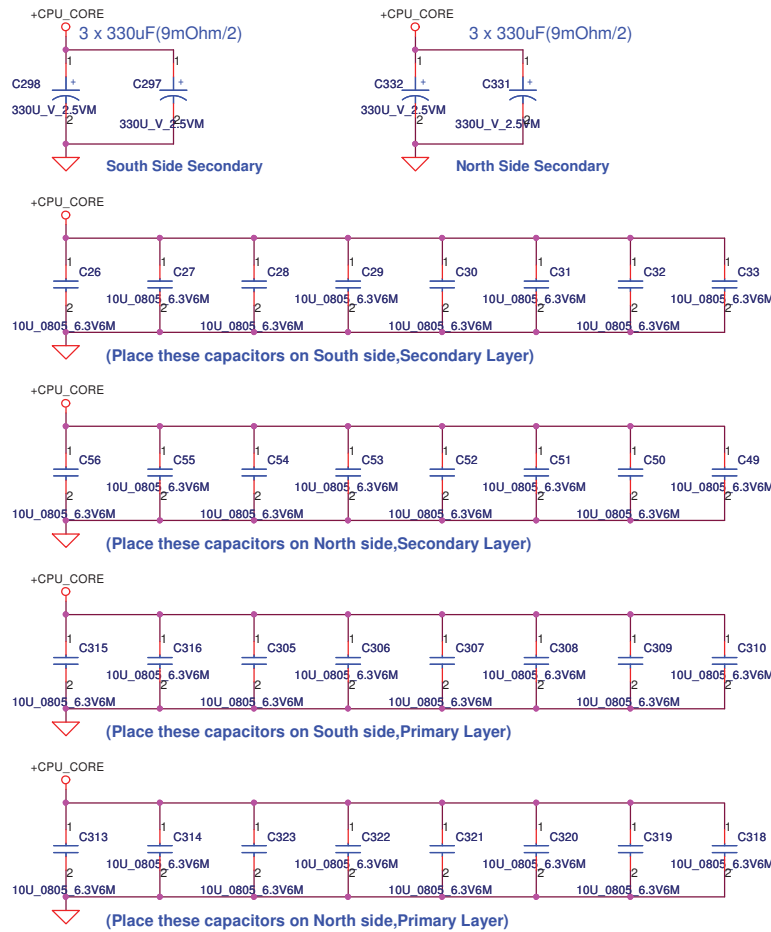
Close to CPU pin
within 500mils.

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								Merom (2/3)			
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								LA-3861P		0.1	
						Date:		Monday, August 20, 2007		Sheet 5 of 47	

JP15D			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA11
D16	VSS[031]	VSS[112]	AA14
D19	VSS[032]	VSS[113]	AA16
D23	VSS[033]	VSS[114]	AA19
D26	VSS[034]	VSS[115]	AA22
E3	VSS[035]	VSS[116]	AA25
E6	VSS[036]	VSS[117]	AB1
E8	VSS[037]	VSS[118]	AB4
E11	VSS[038]	VSS[119]	AB8
E14	VSS[039]	VSS[120]	AB11
E16	VSS[040]	VSS[121]	AB13
E19	VSS[041]	VSS[122]	AB16
E24	VSS[042]	VSS[123]	AB19
F5	VSS[043]	VSS[124]	AB23
F8	VSS[044]	VSS[125]	AB26
F11	VSS[045]	VSS[126]	AC3
F13	VSS[046]	VSS[127]	AC6
F16	VSS[047]	VSS[128]	AC8
F19	VSS[048]	VSS[129]	AC11
F22	VSS[049]	VSS[130]	AC14
F2	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
G4	VSS[052]	VSS[133]	AC21
G1	VSS[053]	VSS[134]	AC24
G23	VSS[054]	VSS[135]	AD2
G26	VSS[055]	VSS[136]	AD5
H3	VSS[056]	VSS[137]	AD8
H6	VSS[057]	VSS[138]	AD11
H21	VSS[058]	VSS[139]	AD13
H24	VSS[059]	VSS[140]	AD16
J2	VSS[060]	VSS[141]	AD19
J5	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD25
J25	VSS[063]	VSS[144]	AE1
K1	VSS[064]	VSS[145]	AE4
K4	VSS[065]	VSS[146]	AE8
K23	VSS[066]	VSS[147]	AE11
K26	VSS[067]	VSS[148]	AE14
L3	VSS[068]	VSS[149]	AE16
L6	VSS[069]	VSS[150]	AE19
L21	VSS[070]	VSS[151]	AE23
L24	VSS[071]	VSS[152]	AE26
M2	VSS[072]	VSS[153]	A2
M5	VSS[073]	VSS[154]	AF6
M22	VSS[074]	VSS[155]	AF8
M25	VSS[075]	VSS[156]	AF11
N1	VSS[076]	VSS[157]	AF13
N4	VSS[077]	VSS[158]	AF16
N23	VSS[078]	VSS[159]	AF19
N26	VSS[079]	VSS[160]	AF21
P3	VSS[080]	VSS[161]	A25
	VSS[081]	VSS[162]	AF25
		VSS[163]	

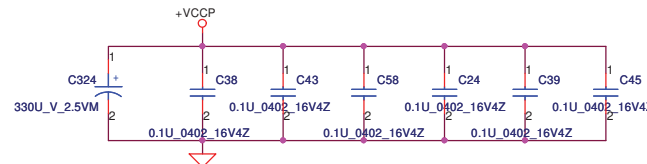
FOX_PZ4782A-274M-41_Merom

ME@



9/25 10U checked. OK for use!

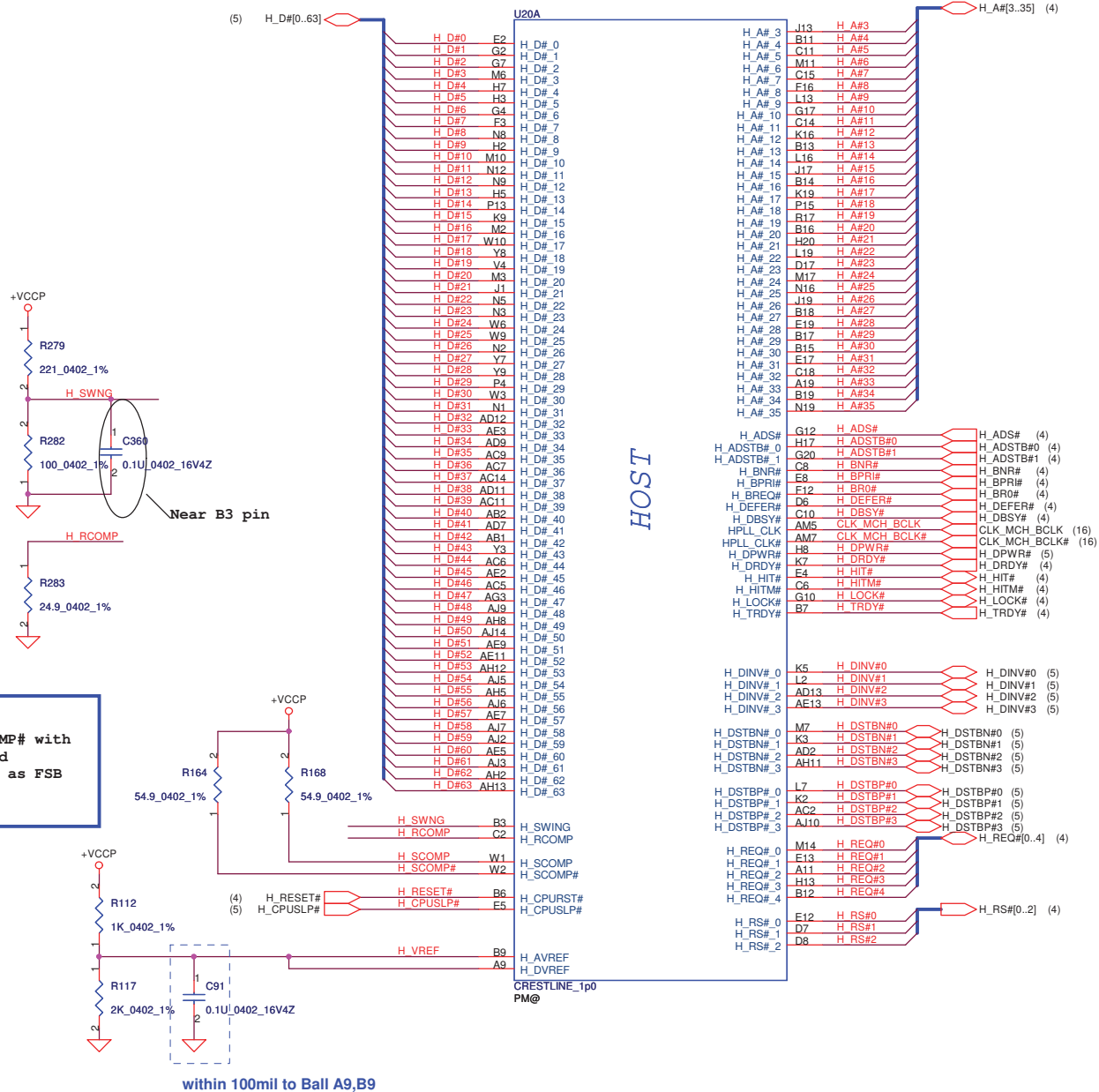
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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								Size B			
								Document Number			
								LA-3861P			
								Date:			
								Monday, August 20, 2007			
								Sheet 6 of 47			

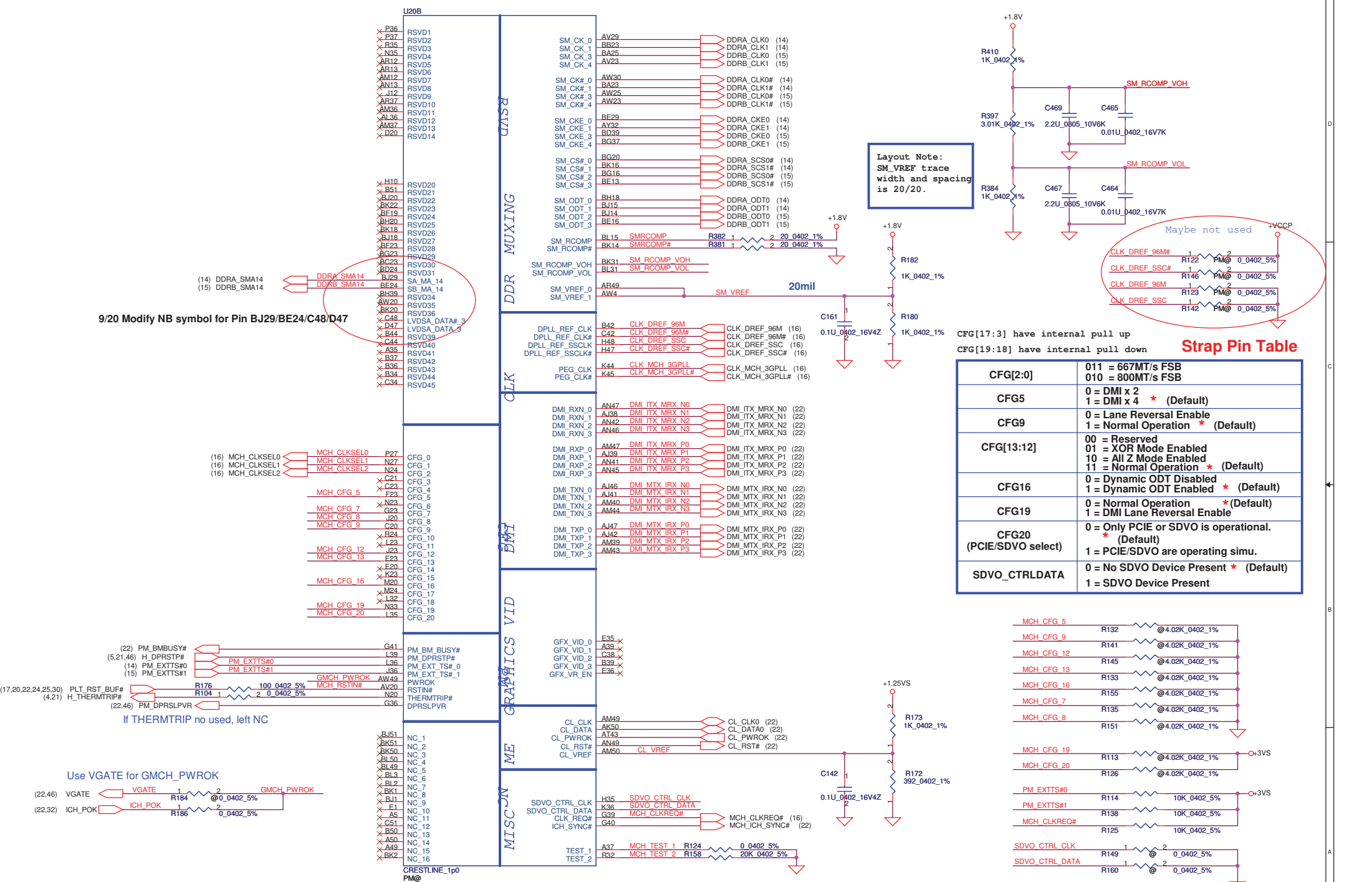
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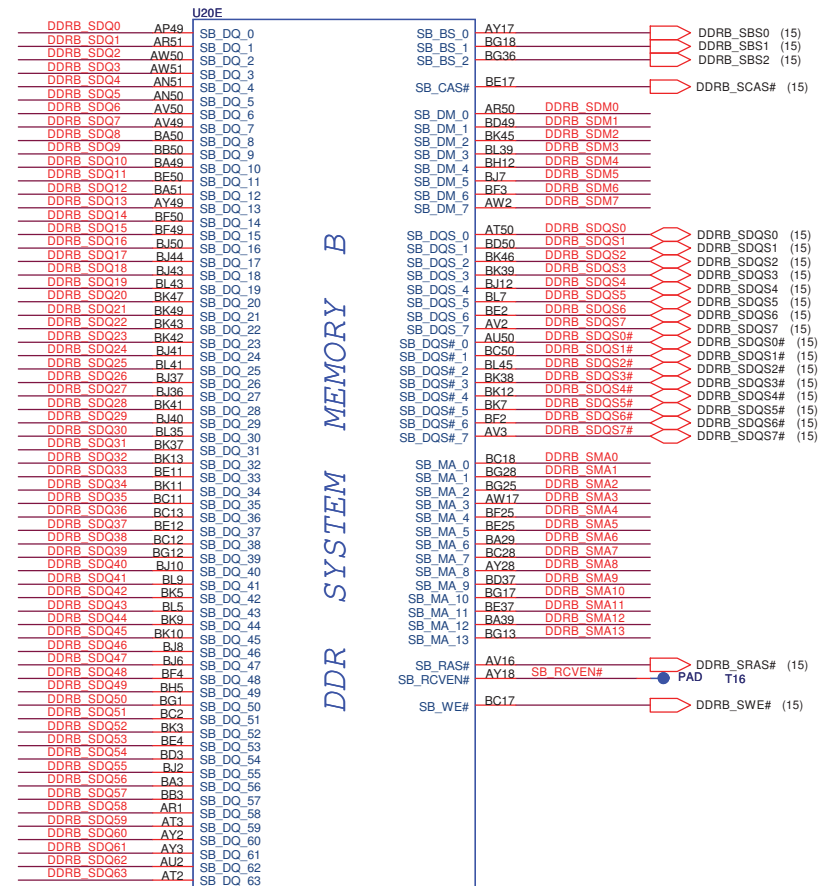
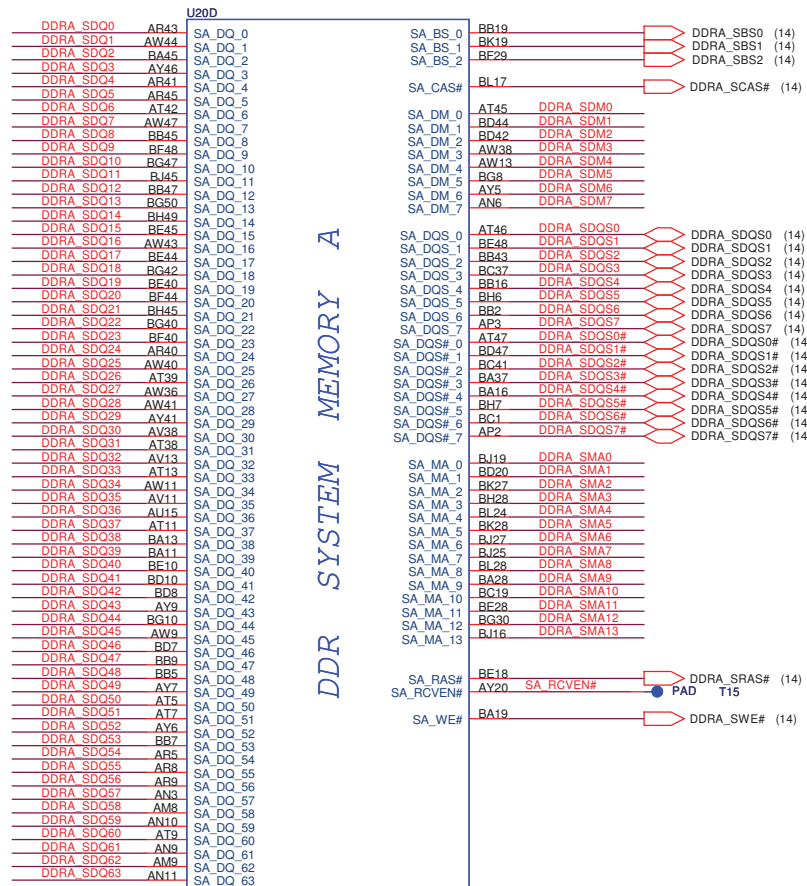
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		Size B	Document Number LA-3861P						Rev 0.1
		Date:	Monday, August 20, 2007			Sheet	7	of	47

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



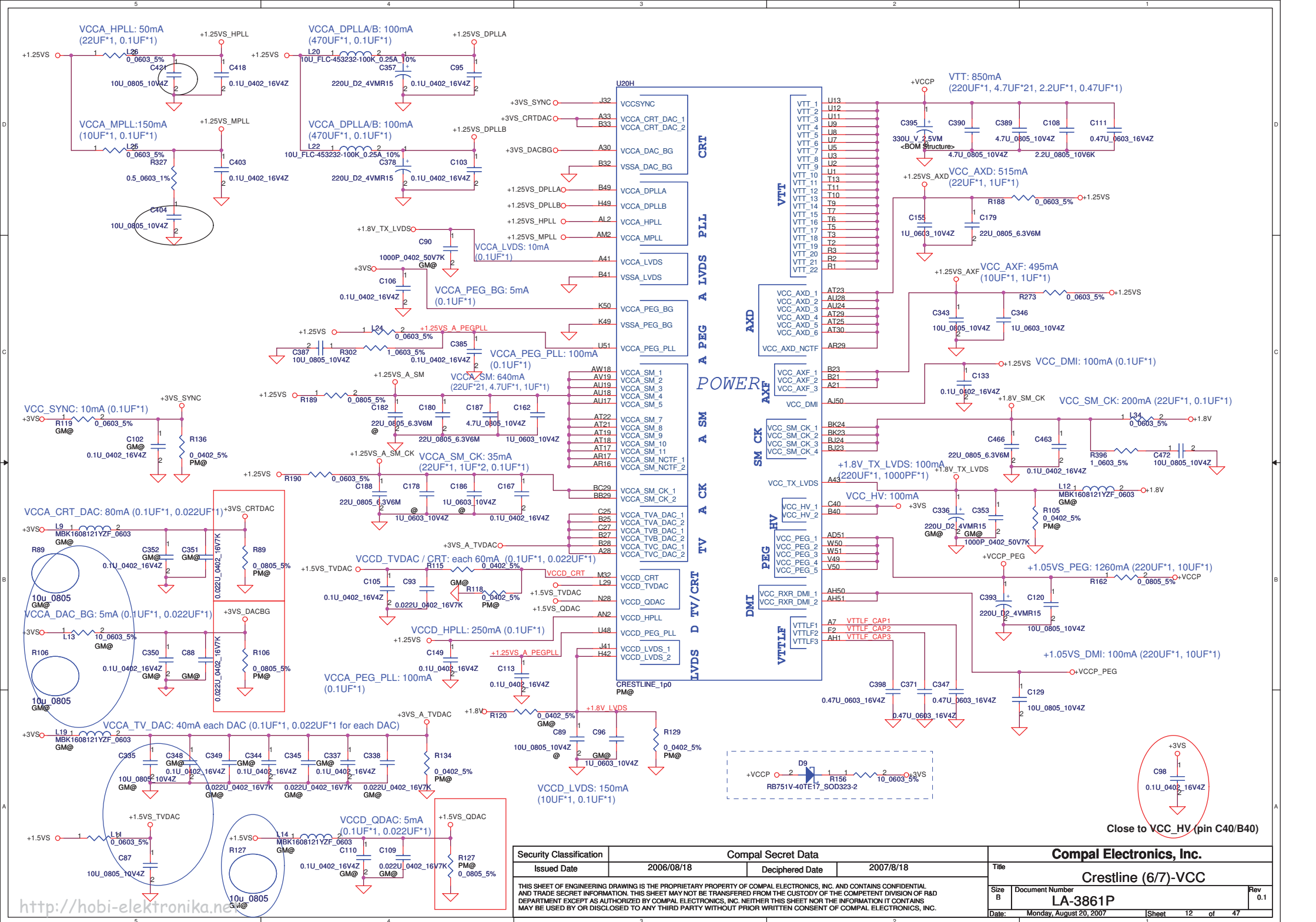


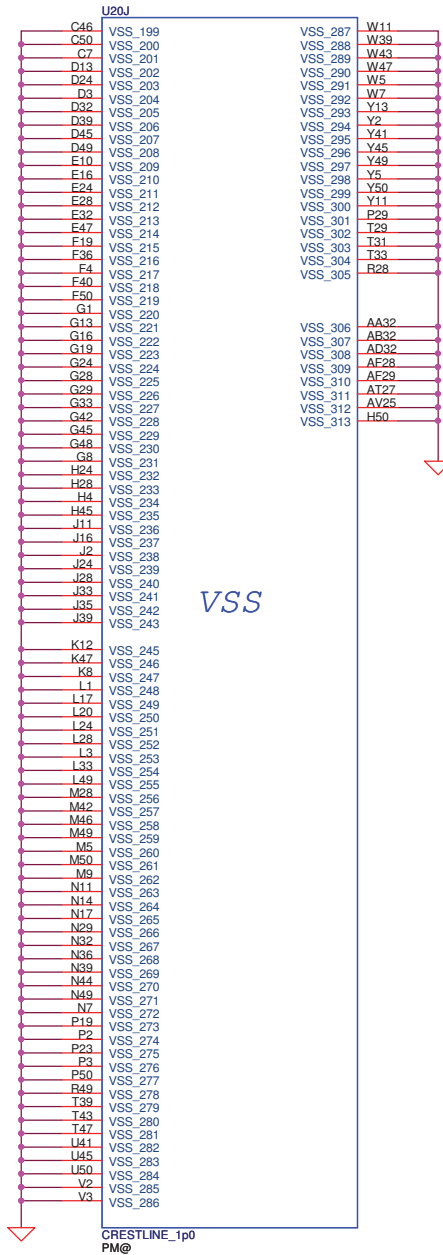
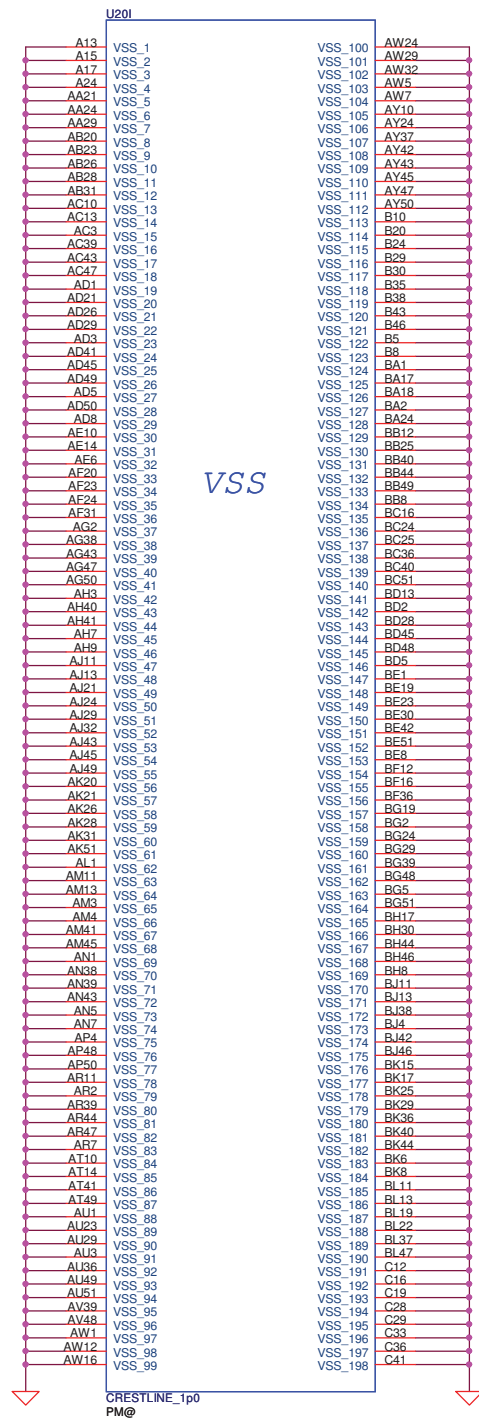
CRESTLINE_1p0
PM@

CRESTLINE_1p0
PM@

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				Crestline (3/7)-DDRII			
				Size B		Document Number	
				LA-3861P			
Date:				Monday, August 20, 2007		Sheet 9 of 47	

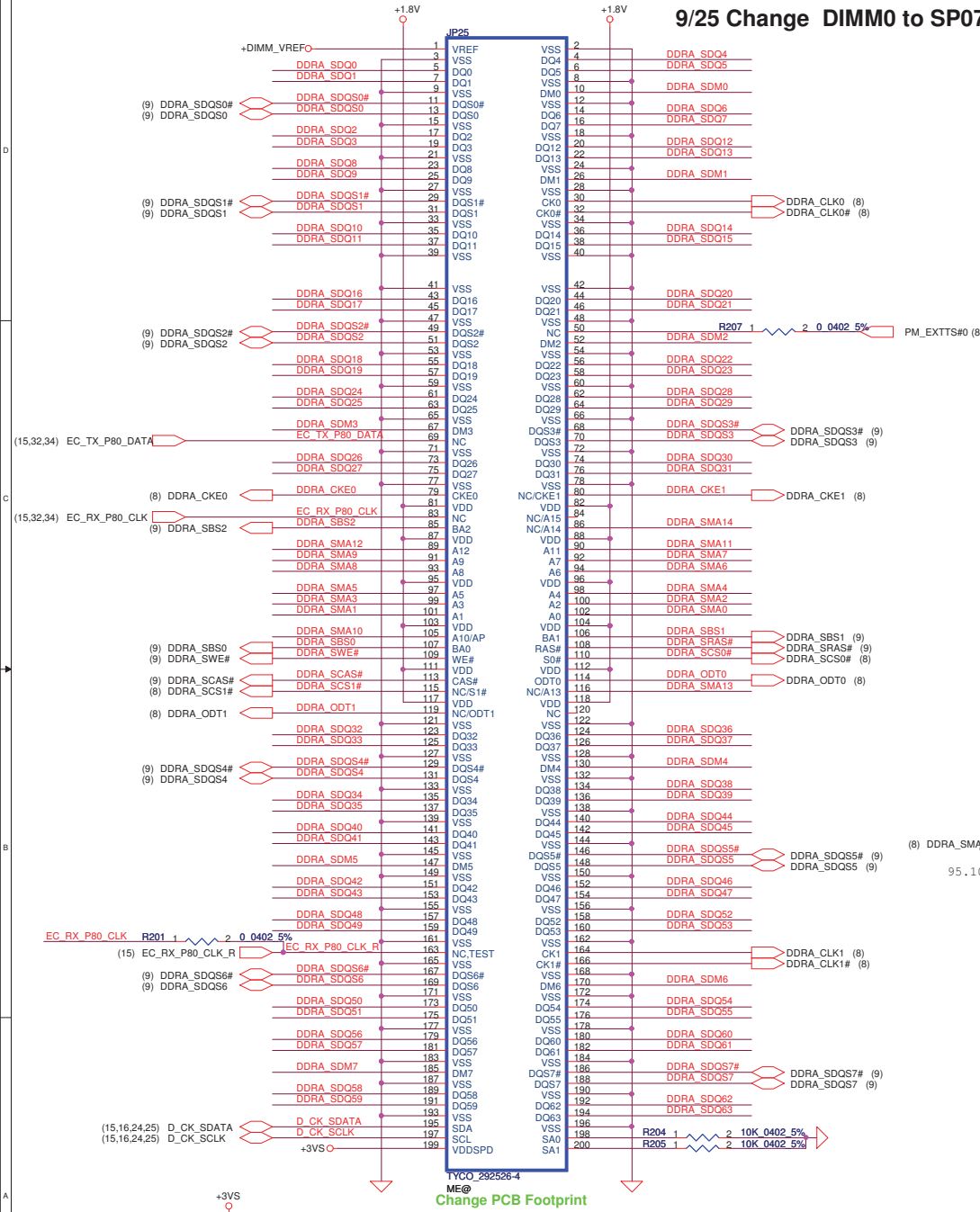




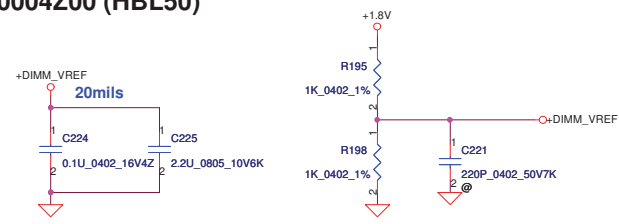


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							LA-3861P			0.1
						Date:	Monday, August 20, 2007		Sheet	13

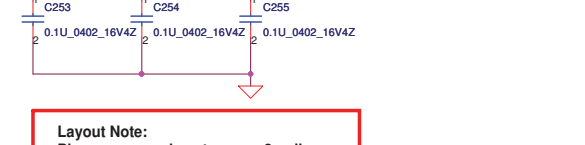
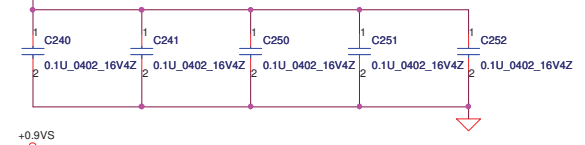
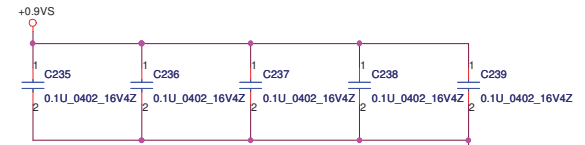
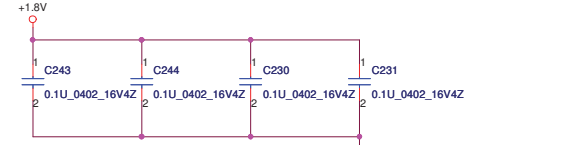
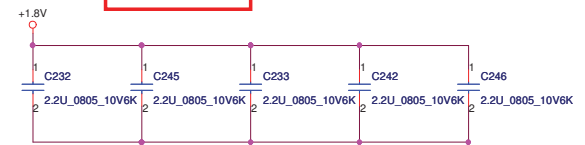
9/25 Change DIMM0 to SP070004Z00 (HBL50)



DIMM0 STD H:5.2mm (BOT)

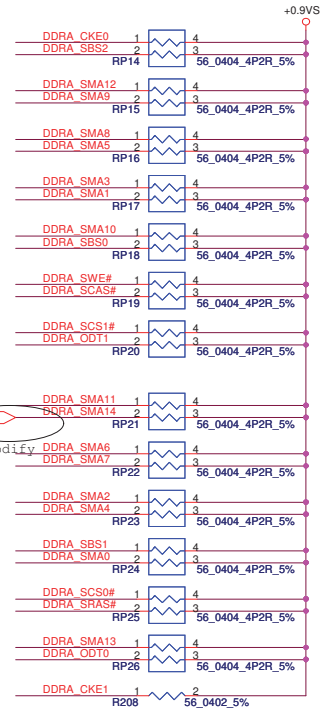


Layout Note:
Place near JP35



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

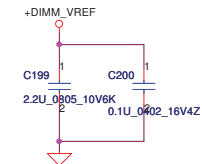
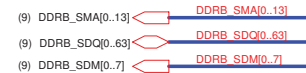
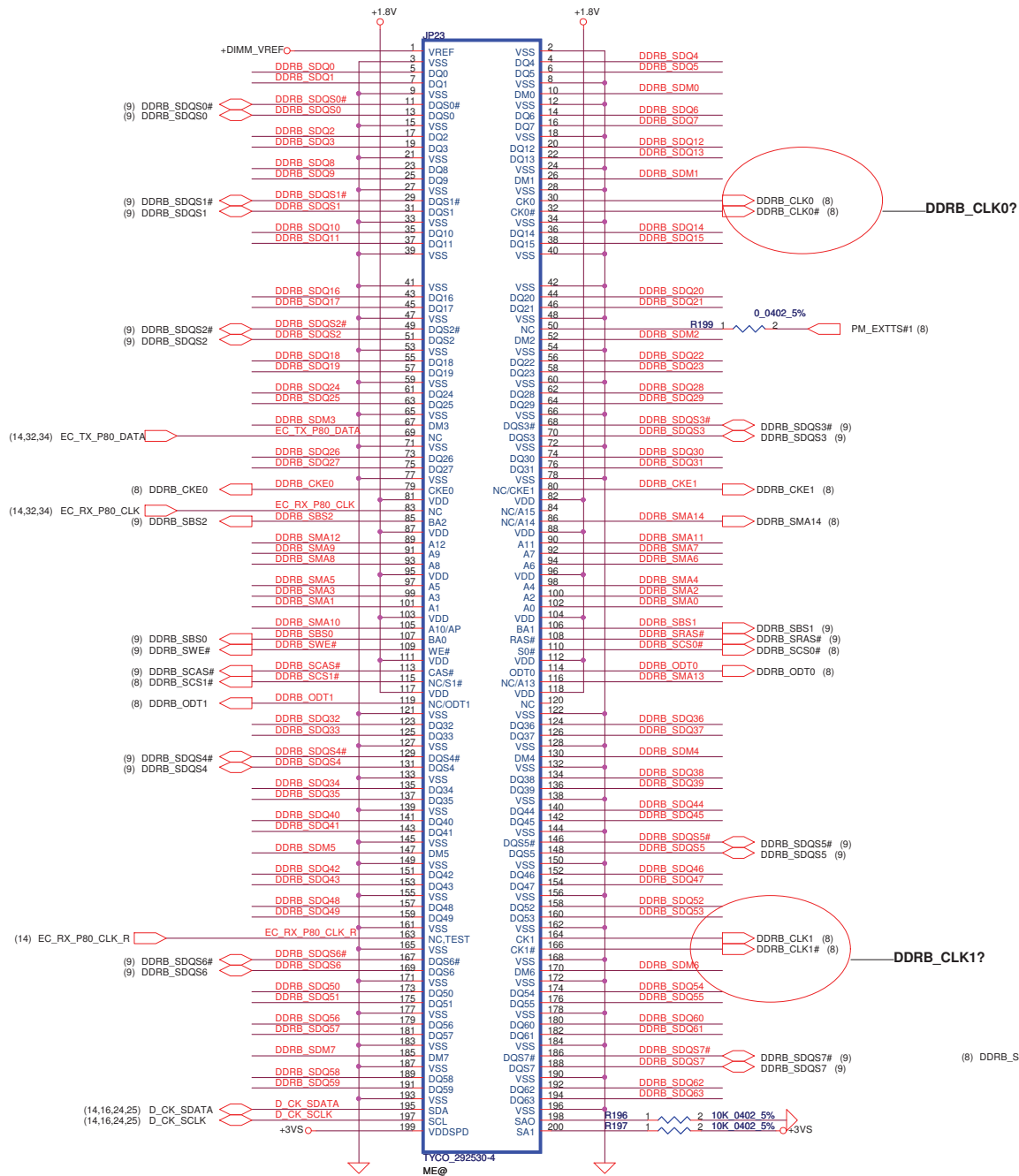
- (9) DDR_A_SMA[0..13] < DDR_A_SMA[0..13]
- (9) DDR_A_SQ[0..63] < DDR_A_SQ[0..63]
- (9) DDR_A_SDM[0..7] < DDR_A_SDM[0..7]



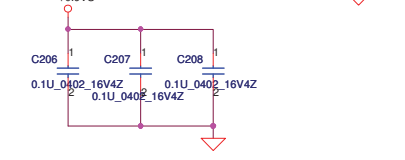
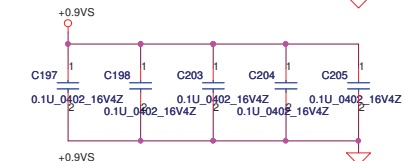
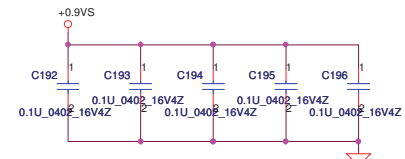
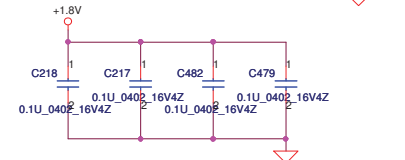
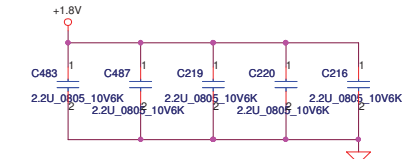
Layout Note:
Place these resistor closely JP35,all trace length Max=1.5"

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				DDR II-SODIMM0	
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				LA-3861P	
				Date:	Monday, August 20, 2007
				Sheet	14 of 47
				Rev	0.1

9/25 Change DIMM1 to SP070006F00



Layout Note:
Place near JP34



Layout Note:
Place these resistor
closely JP35,all
trace length Max=1.5"

Layout Note:
Place one cap close to every 2 p
resistors terminated to +0.9VS

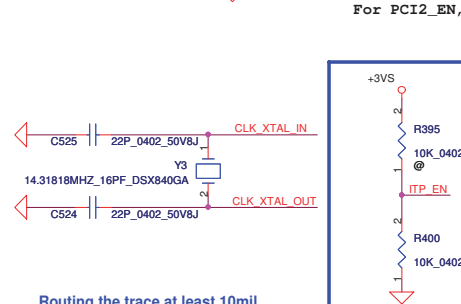
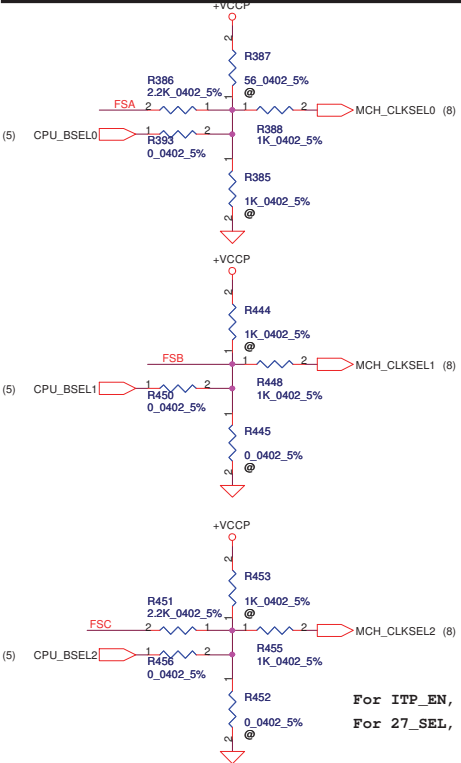
DIMM1 STD H:9.2mm (BOT)

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				LA-3861P	
				Date	Monday, August 20, 2007
				Sheet	15 of 47

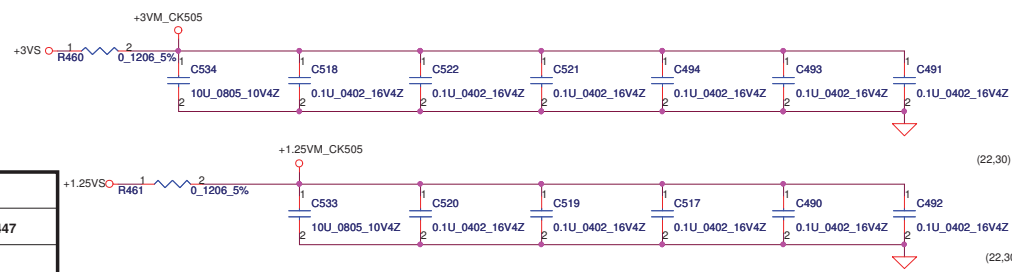
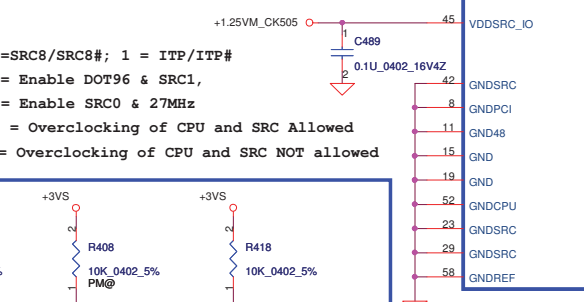
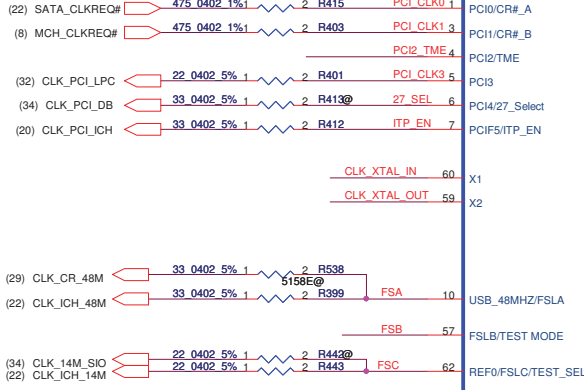
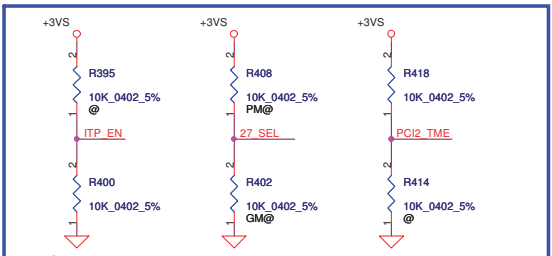
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

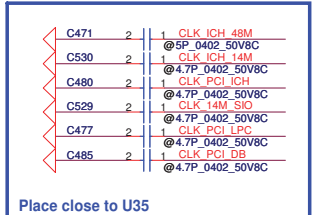
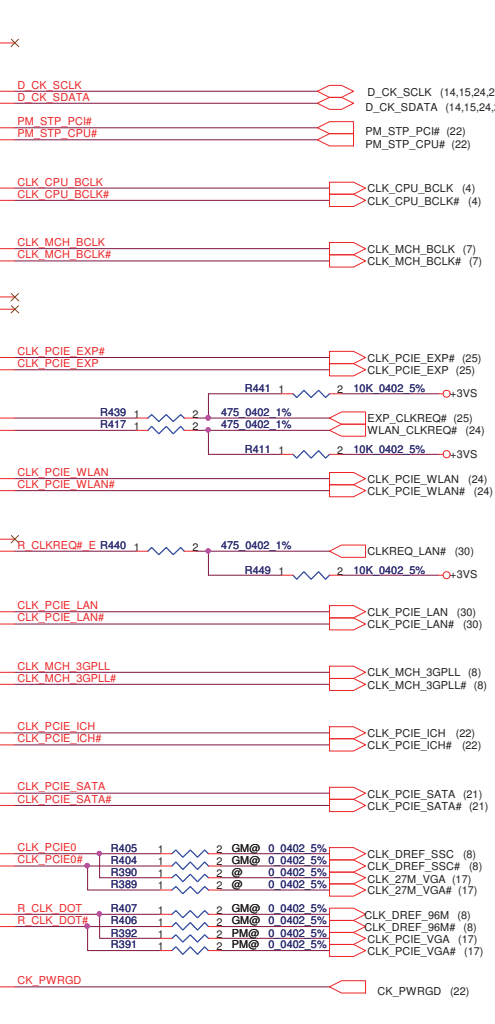
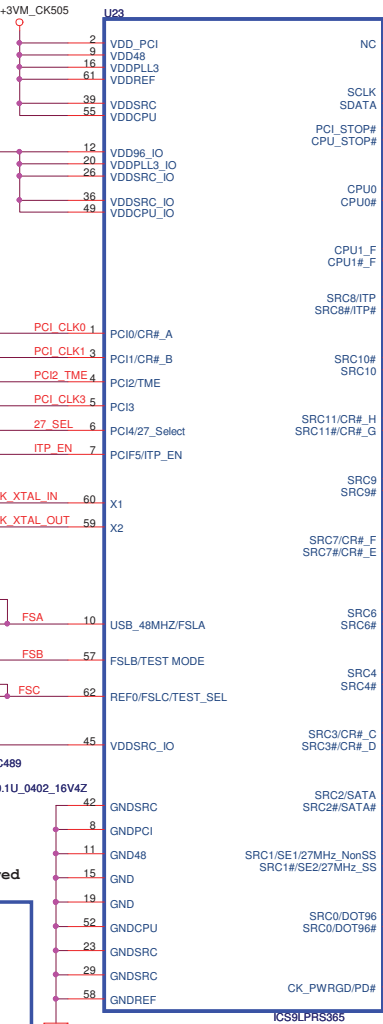
CPU Driven	Stuff						
★ (Default)	No Stuff	R401	R408	R417	R430	R438	R447
	Stuff	R401	R417	R447			
667MHz	No Stuff	R408	R430	R438			
	Stuff	R408	R417	R447			
800MHz	No Stuff	R401	R430	R438			
	Stuff	R401	R417	R447			



For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

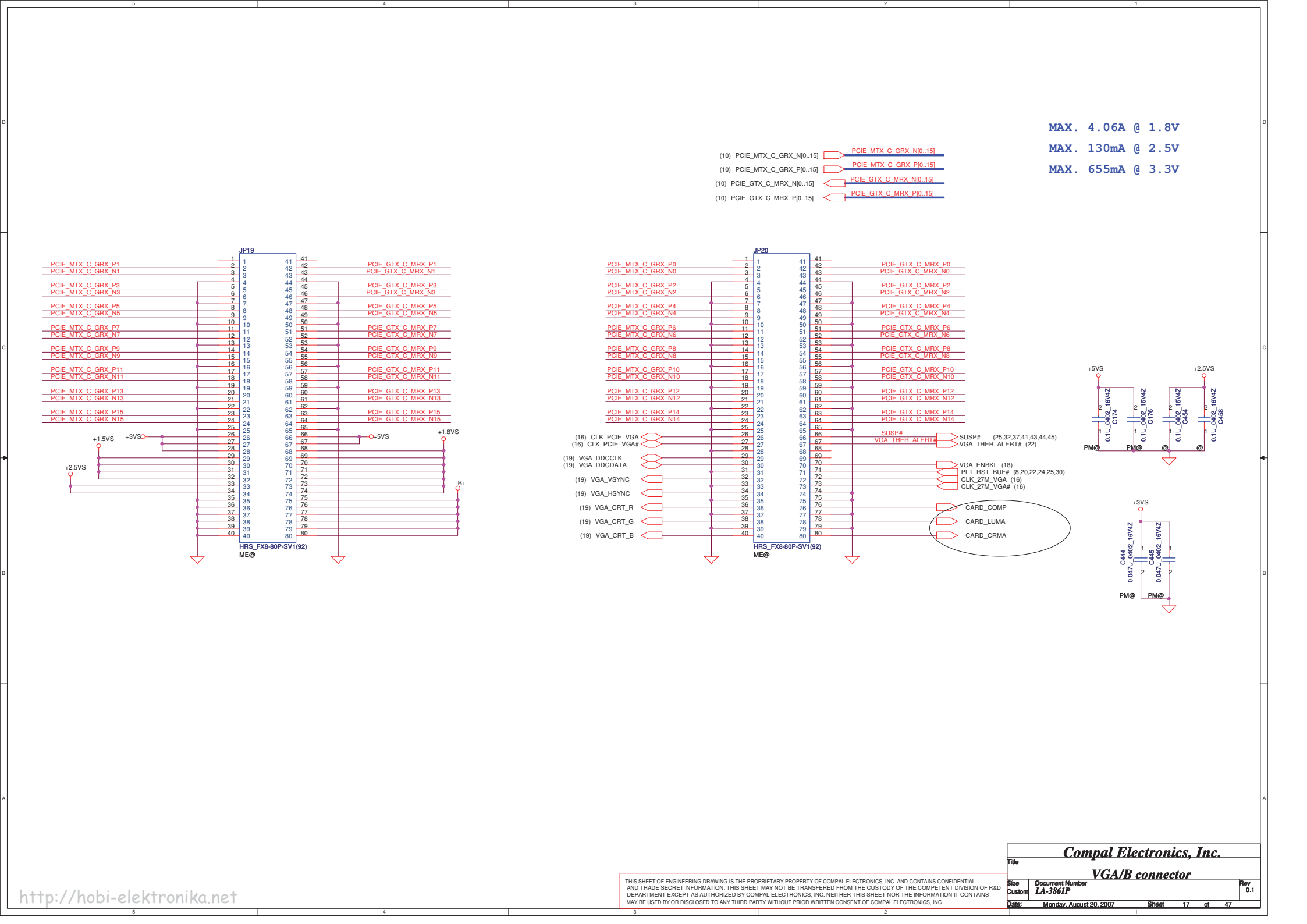


4/16 : Change P/N from SA0001GT10(ICS) to SA00001J00 (SILEGO)

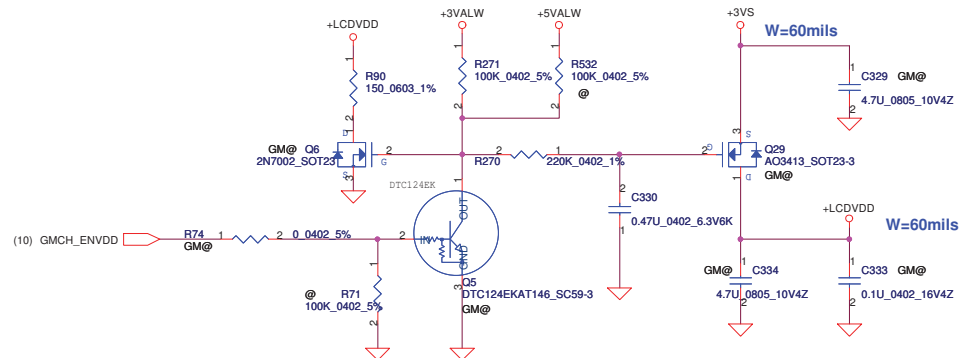


Place close to U35

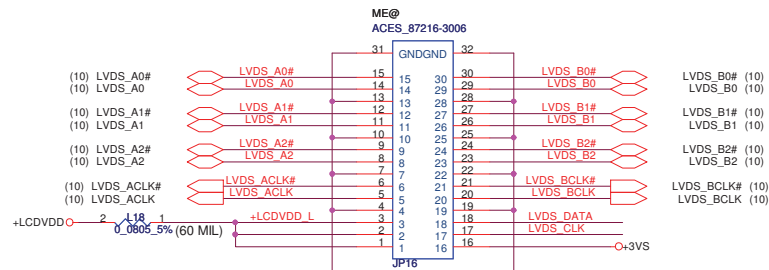
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Clock generator	
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				LA-3861P	Rev 0.1
				Date: Monday, August 20, 2007	Sheet 16 of 47



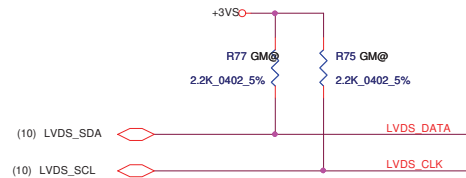
LCD POWER CIRCUIT



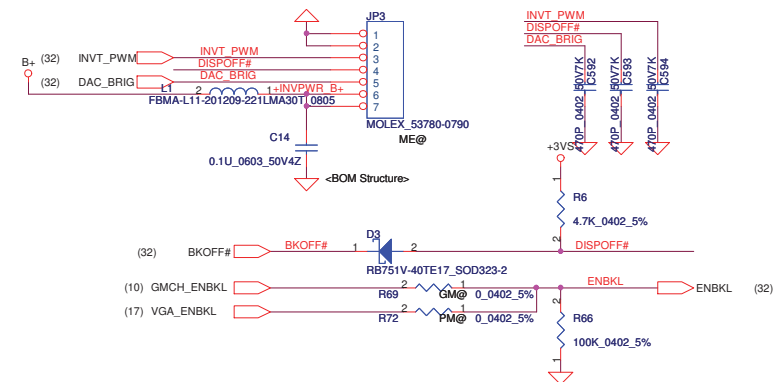
LCD/PANEL BD. Conn.



Follow HEL80's pin definition
Except pin 29



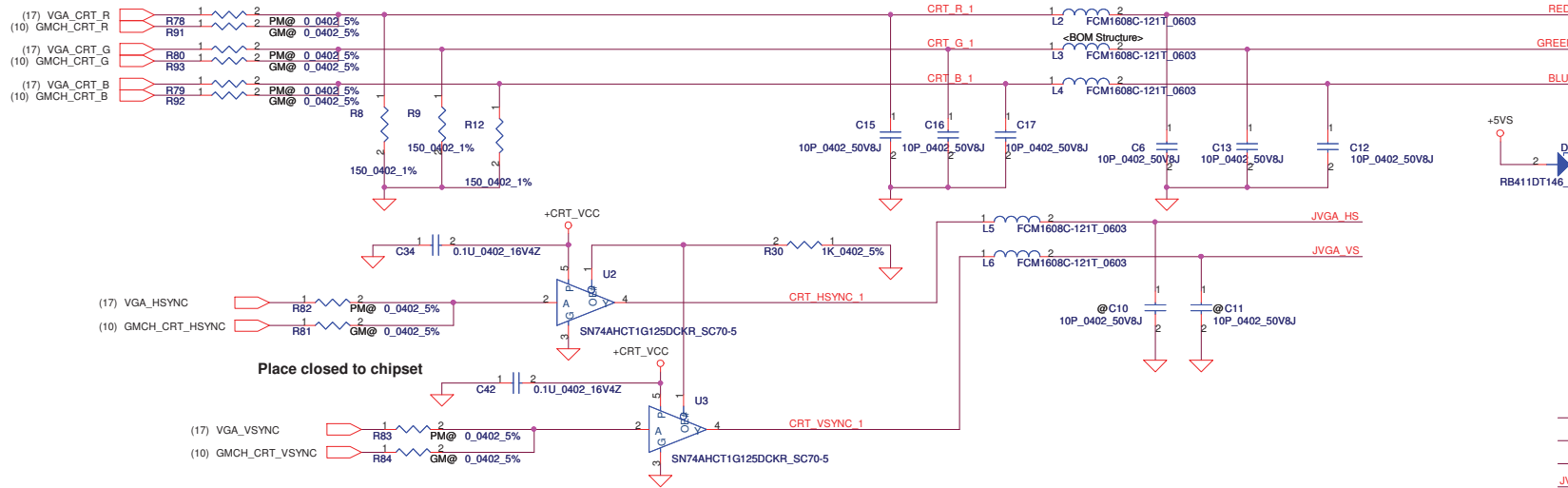
INVERTER Conn.



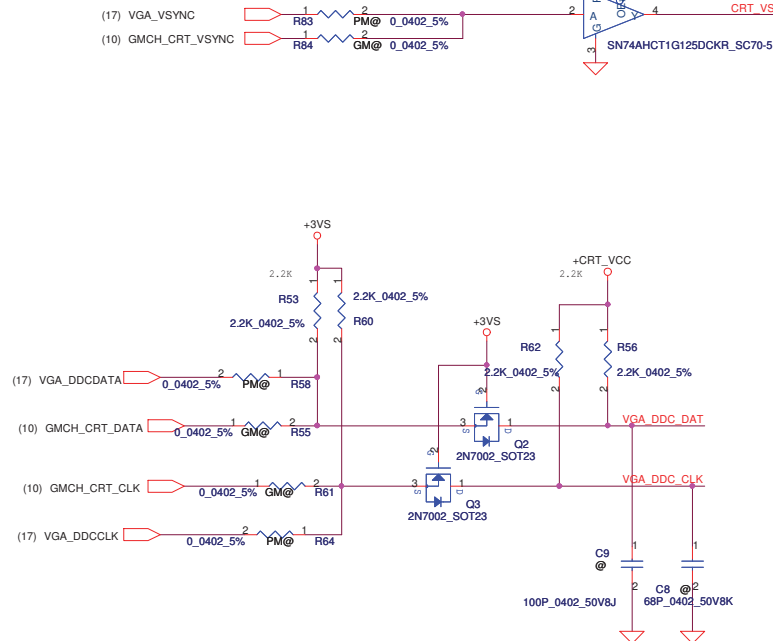
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Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title				
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						Size B	Document Number			LA-3861P		Rev 0.1
						Date	Monday, August 20, 2007			Sheet 18	of 47	

CRT Connector

Place closed to chipset

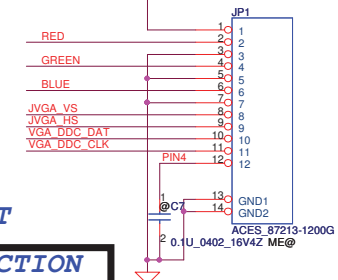


Place closed to chipset

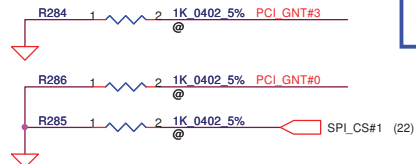
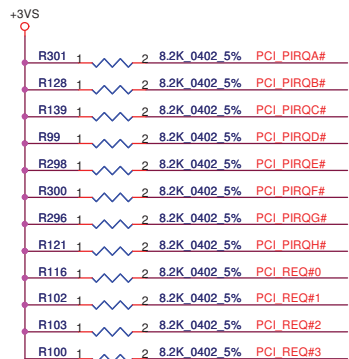
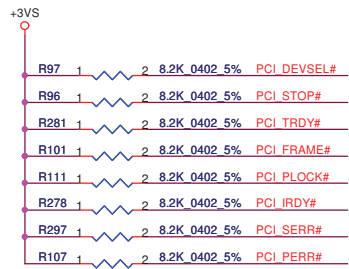


PIN ASSIGMENT

PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSNC
9	13	HSNC
	11	SENSE
10	12	SM_DAT
11	15	SM_CLK
12	4	PIN4



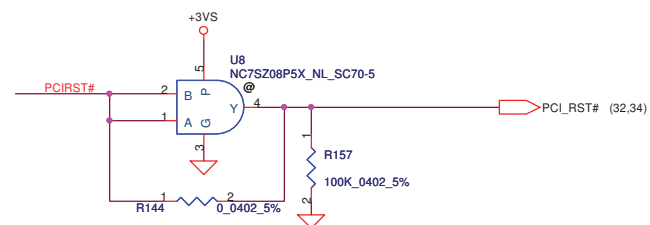
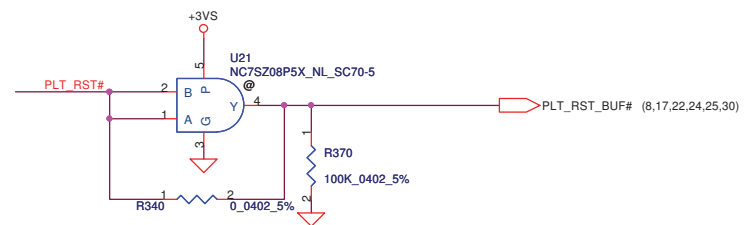
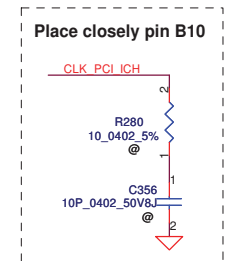
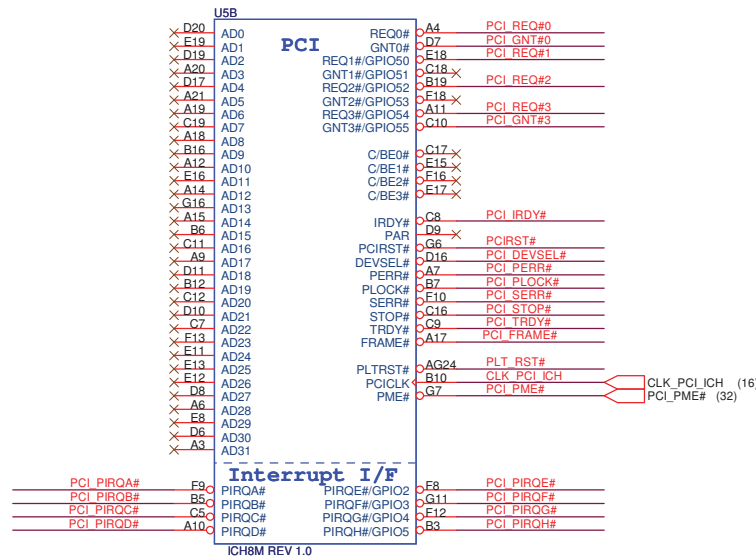
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				LA-3861P	Rev 0.1
				Date: Monday, August 20, 2007	Sheet 19 of 47



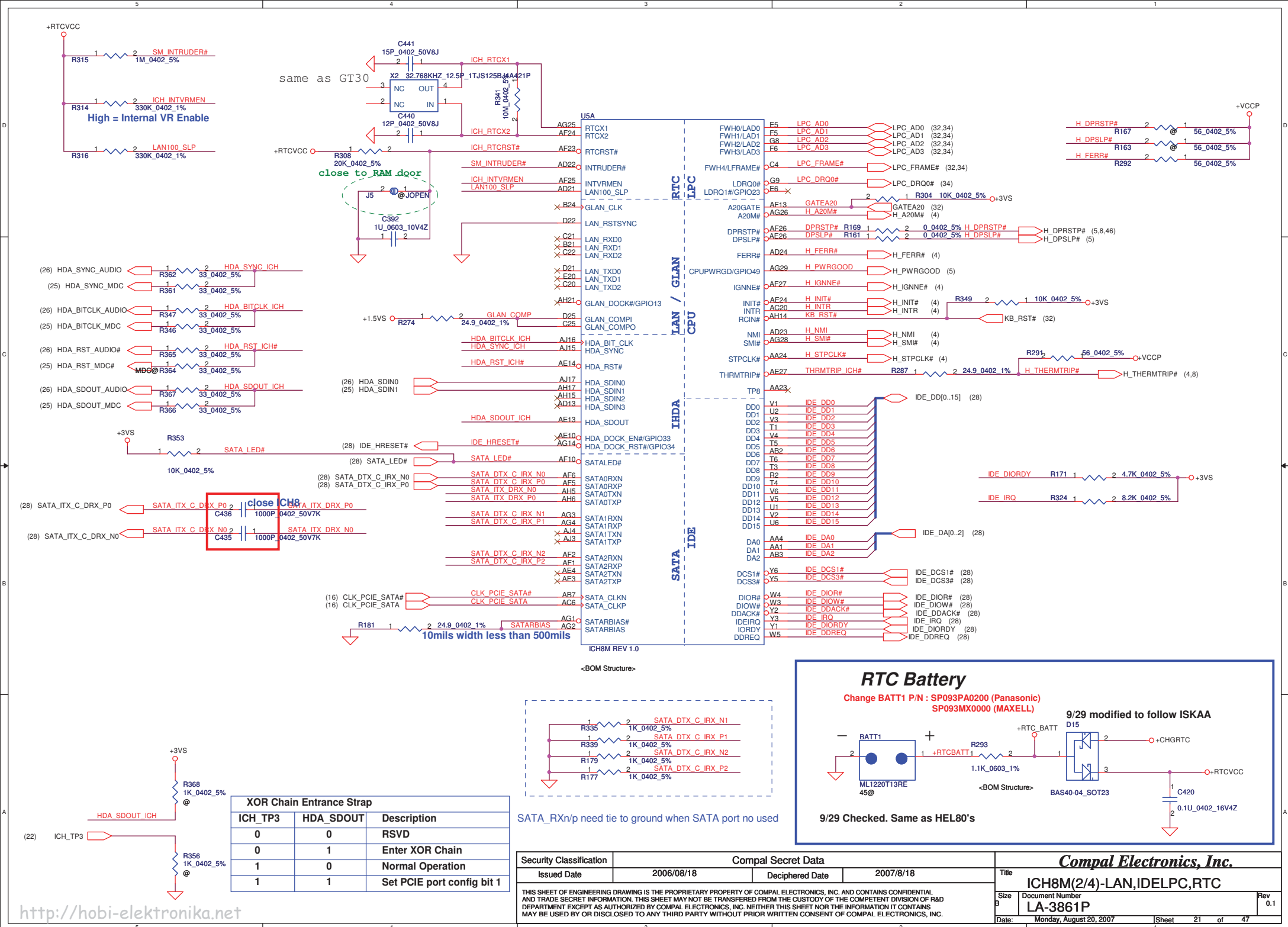
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

10/17 : Change P/N from SA000010G00 to SA00001JU10
 10/17 : FootPrint : SA000010G00
 BOM : SA00001JU10

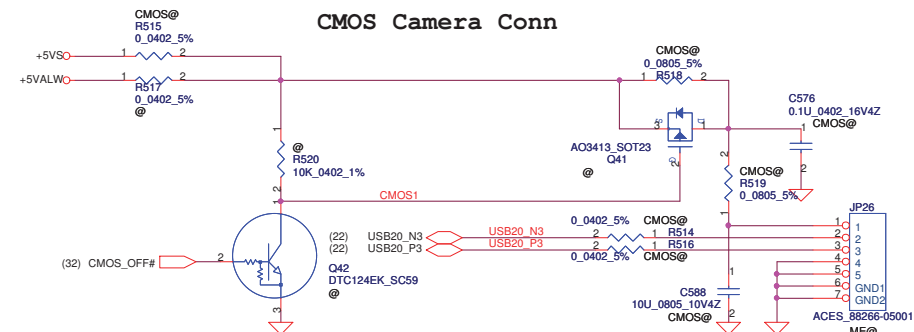
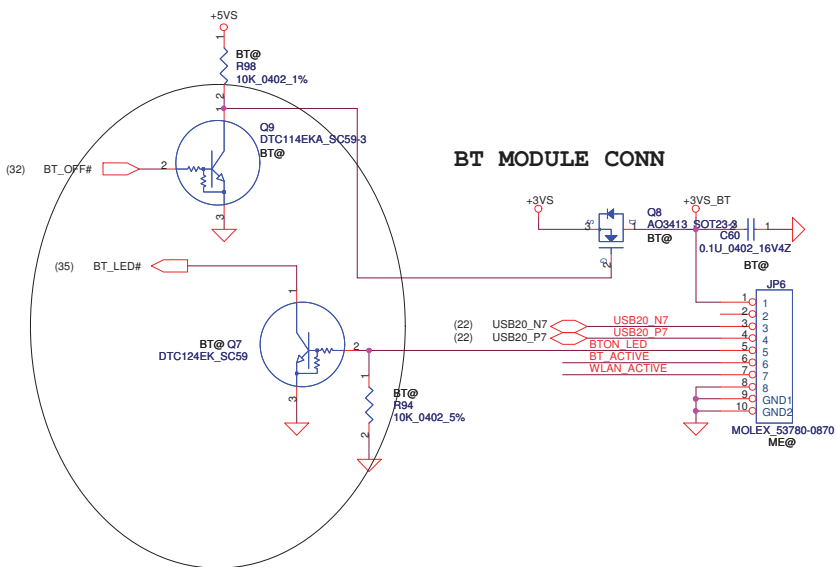
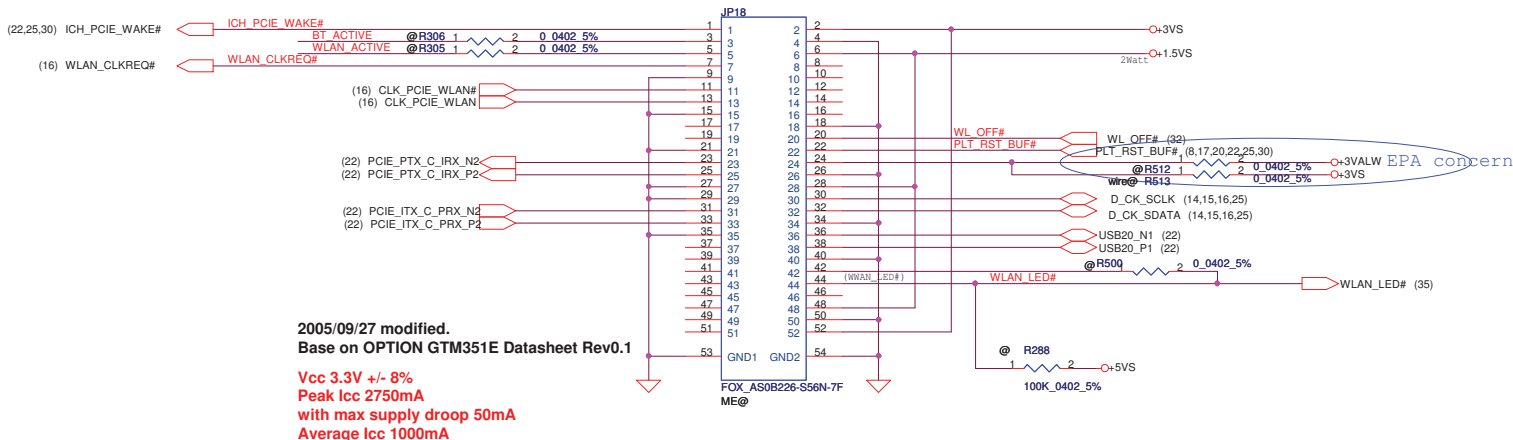
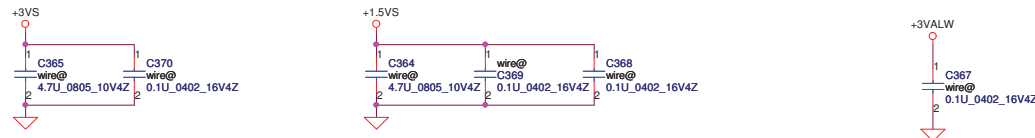


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Size		Document Number		Rev	
		LA-3861P		0.1	
Date:		Monday, August 20, 2007		Sheet 20 of 47	

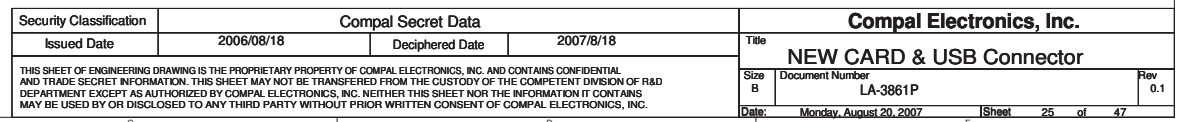
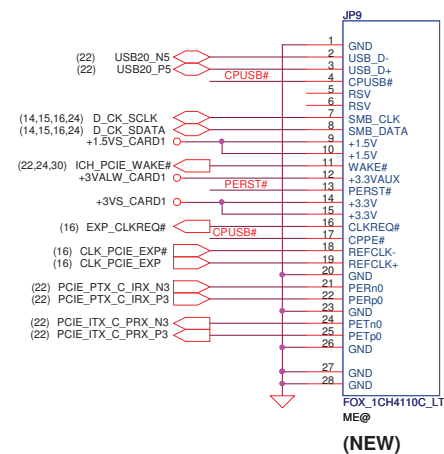
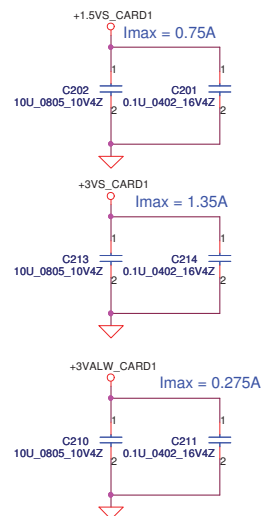


Mini-Express Card for 3G Or TV Tuner

Mini-Express Card for WLAN



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				Size	Document Number
				LA-3861P	
				Date	Rev
				Monday, August 20, 2007	0.1
				Sheet	24 of 47



AC97 Codec

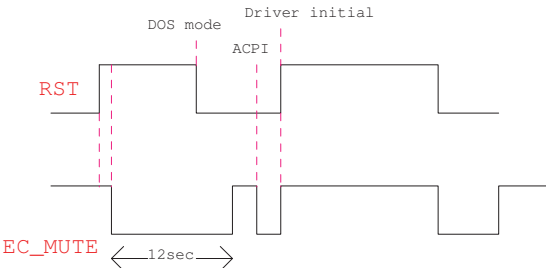
28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)

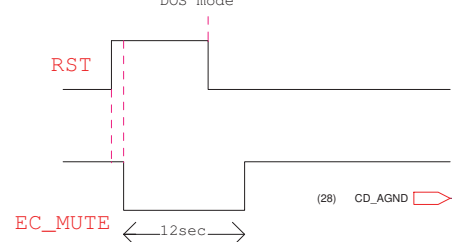
4.85V

SUB WOOFER SUPPORT	
ALC262	
ALC861D	

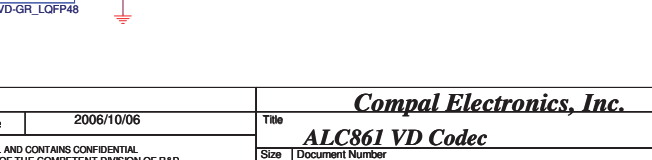
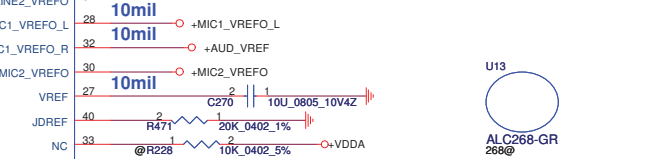
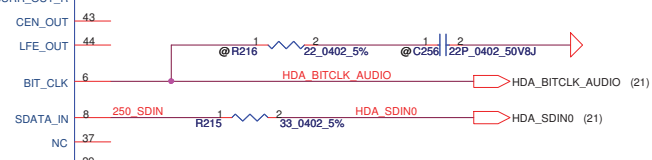
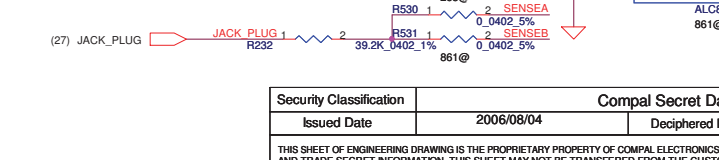
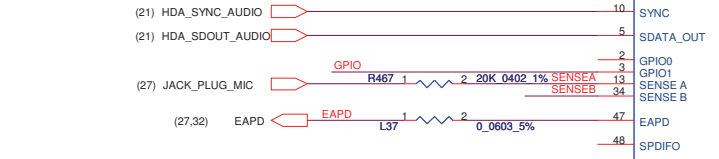
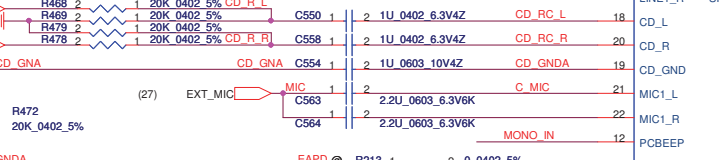
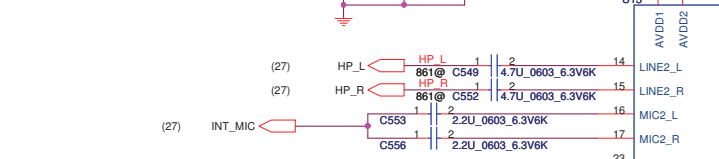
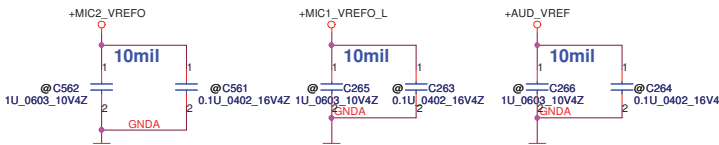
Window mode



DOS mode

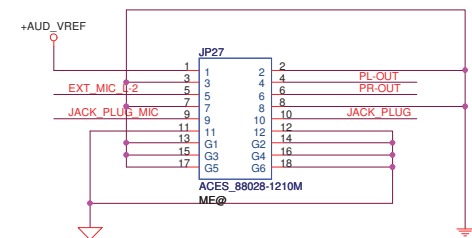
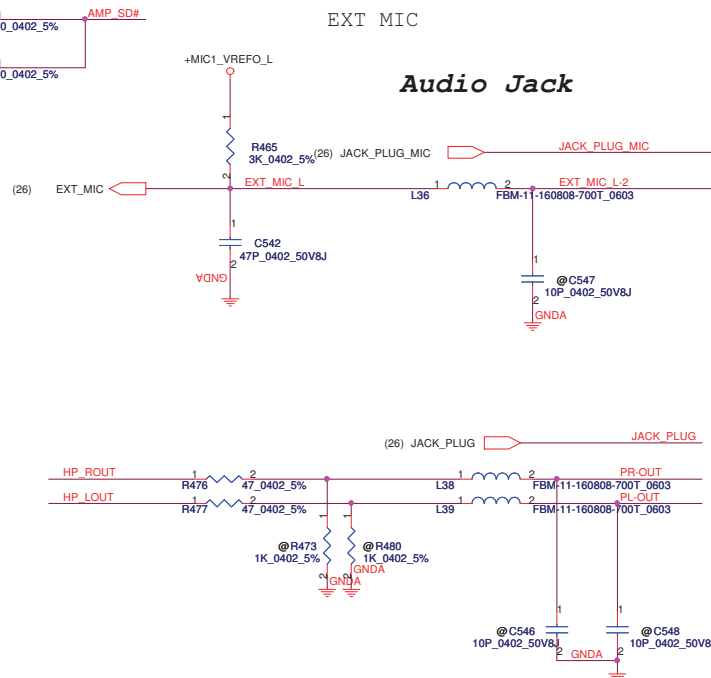
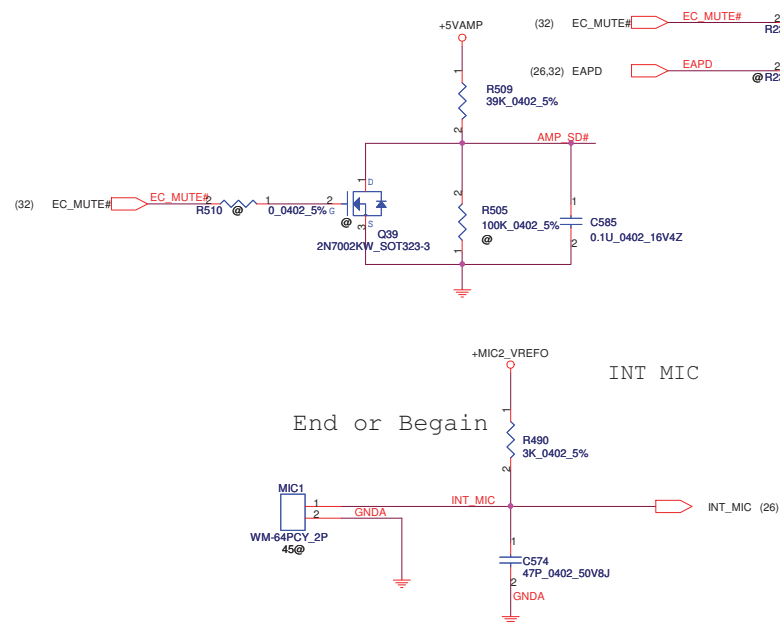
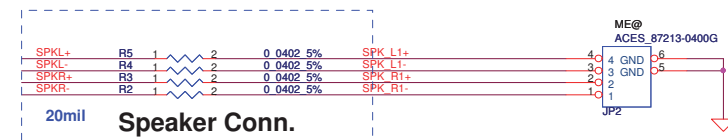
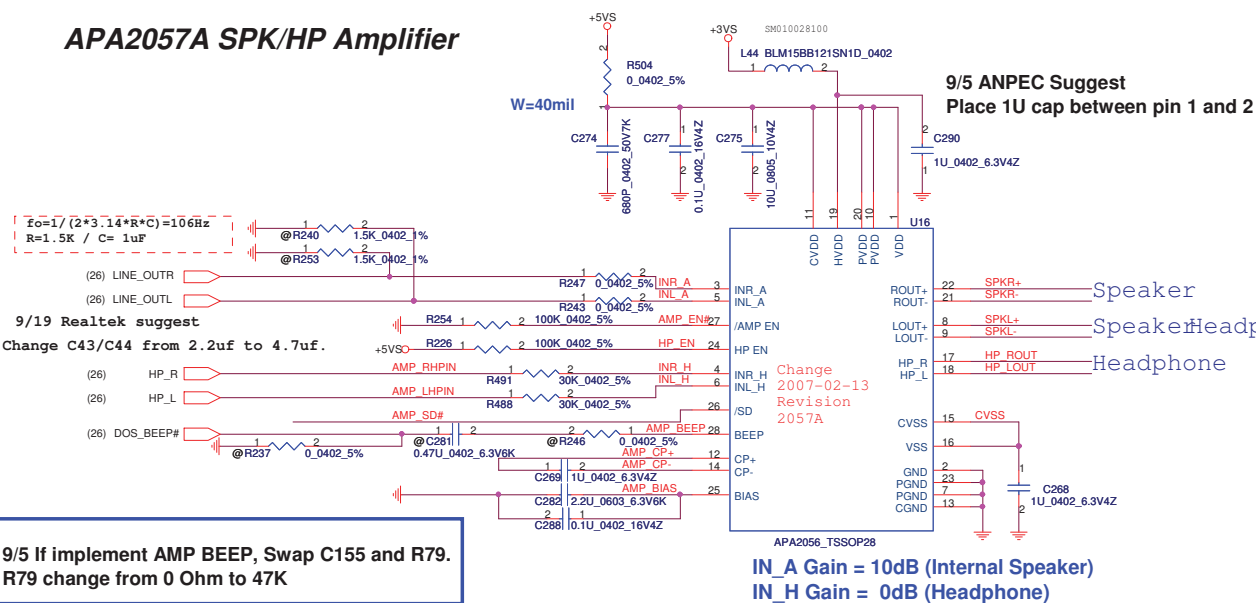


<http://hobi-elektronika.net>

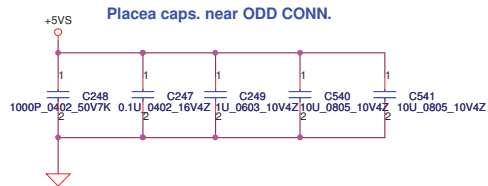


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				Custom	LA-3861P
				Date	Monday, August 20, 2007
				Sheet	26 of 47
				Rev	0.1

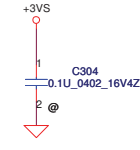
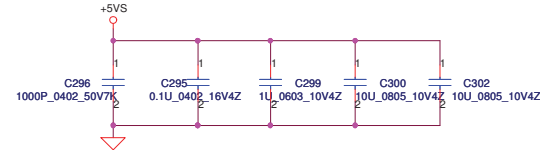
APA2057A SPK/HP Amplifier



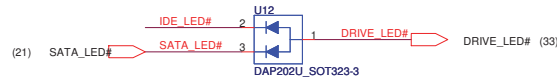
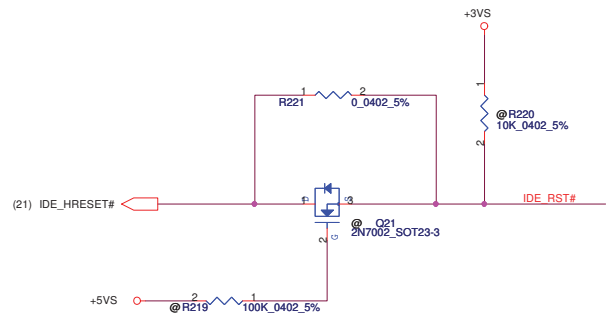
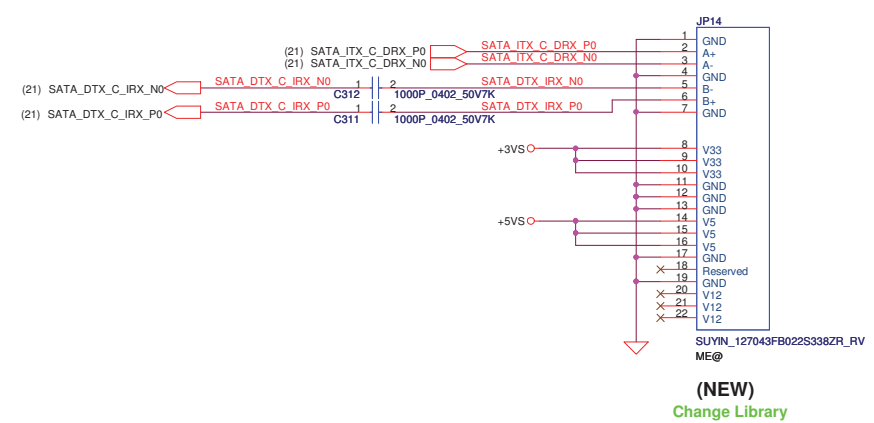
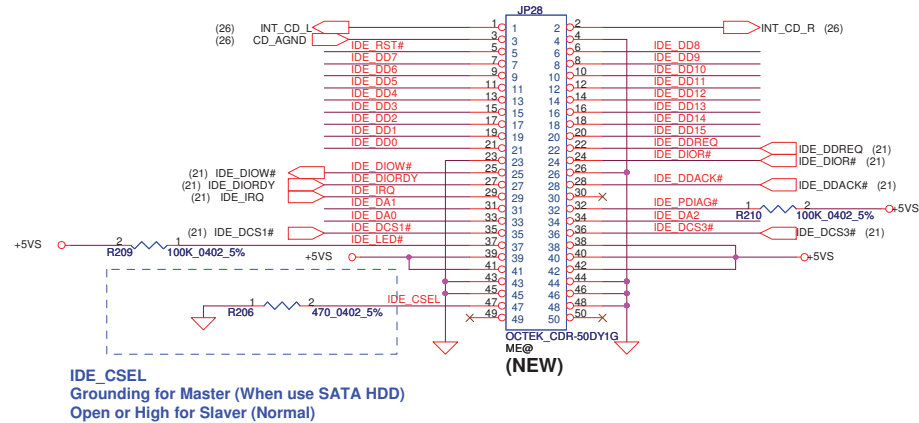
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				Date:	Monday, August 20, 2007	Sheet 27 of 47



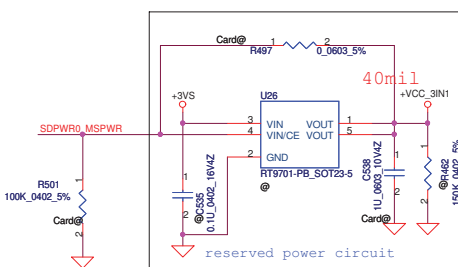
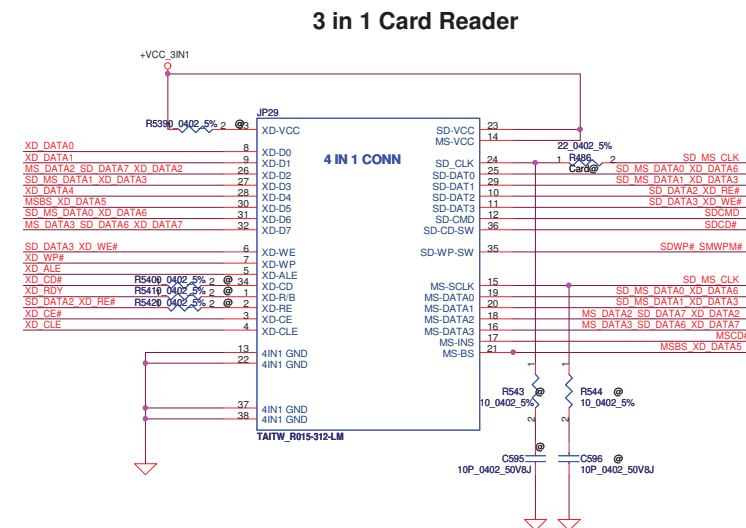
(21) IDE_DD[0..15] IDE_DD[0..15]
 (21) IDE_DA[0..2] IDE_DA[0..2]



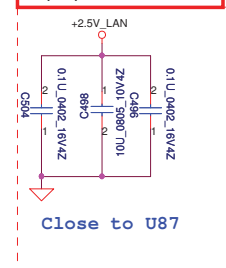
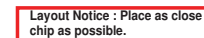
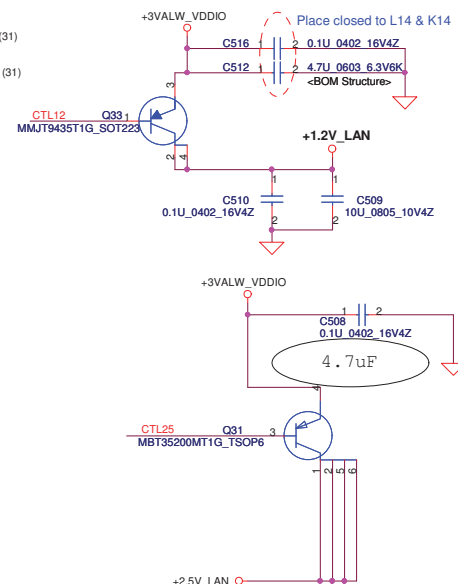
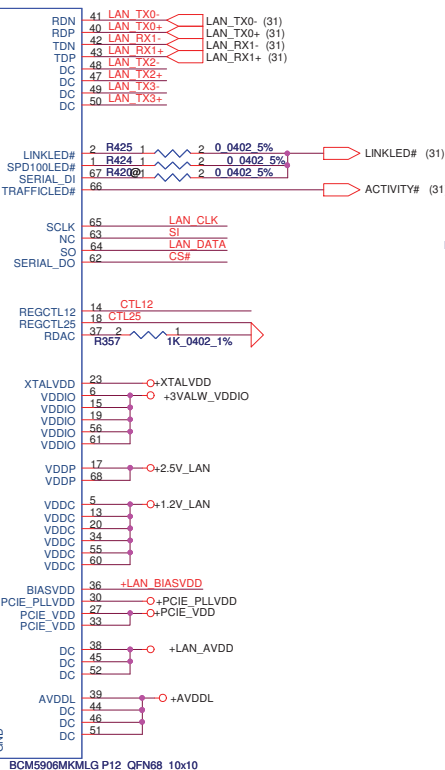
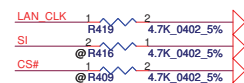
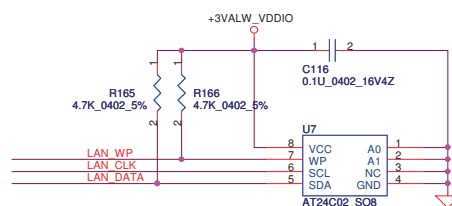
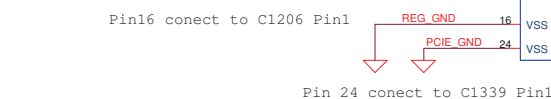
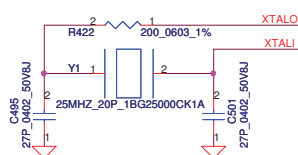
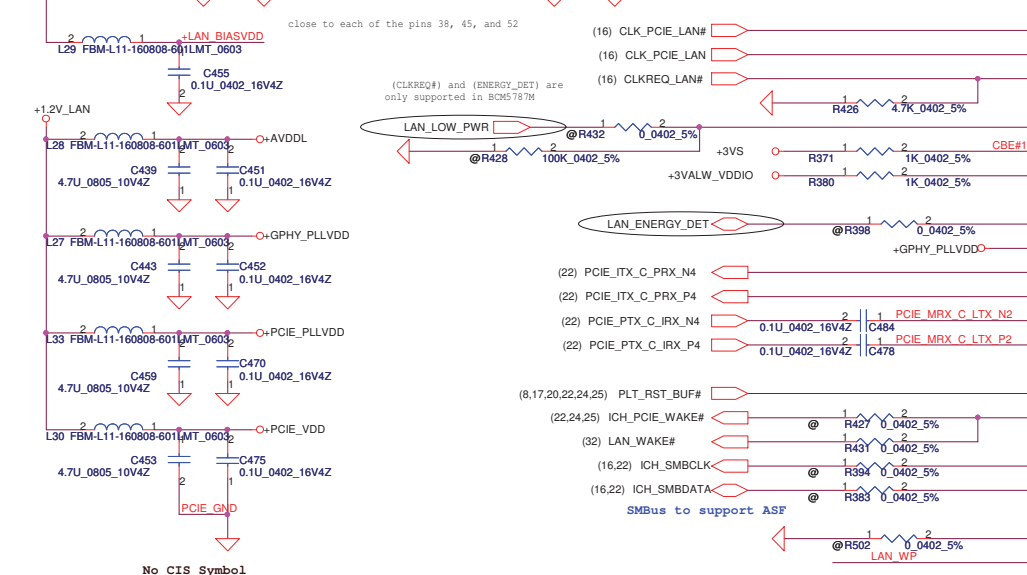
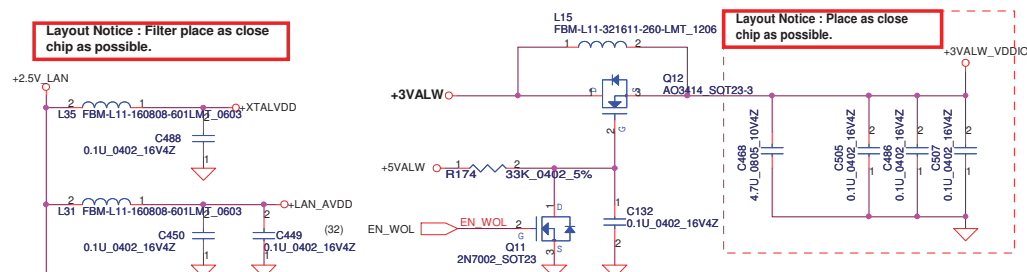
SATA HDD Conn.



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Issued Date				2006/08/18				Deciphered Date			
2006/08/18				2007/8/18				Title			
HDD & ODD Connector				Document Number				Rev			
LA-3861P				0.1				Date			
Monday, August 20, 2007				Sheet				28 of 47			

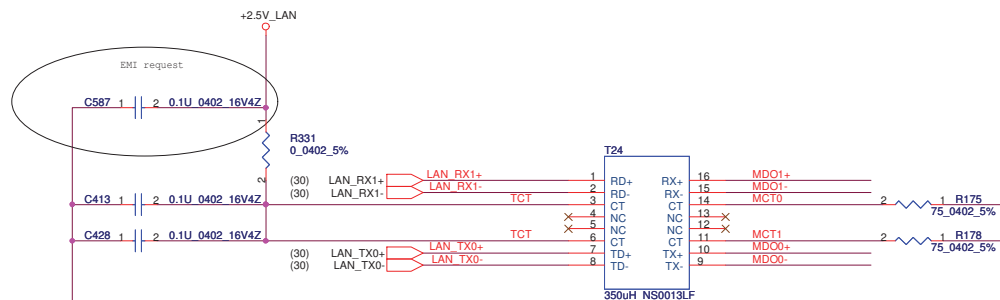


Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> <i>1394+3 in 1 Card</i>	
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				Custom	LA-3861P
				Date:	Monday, August 20, 2007
				Sheet	29 of 47

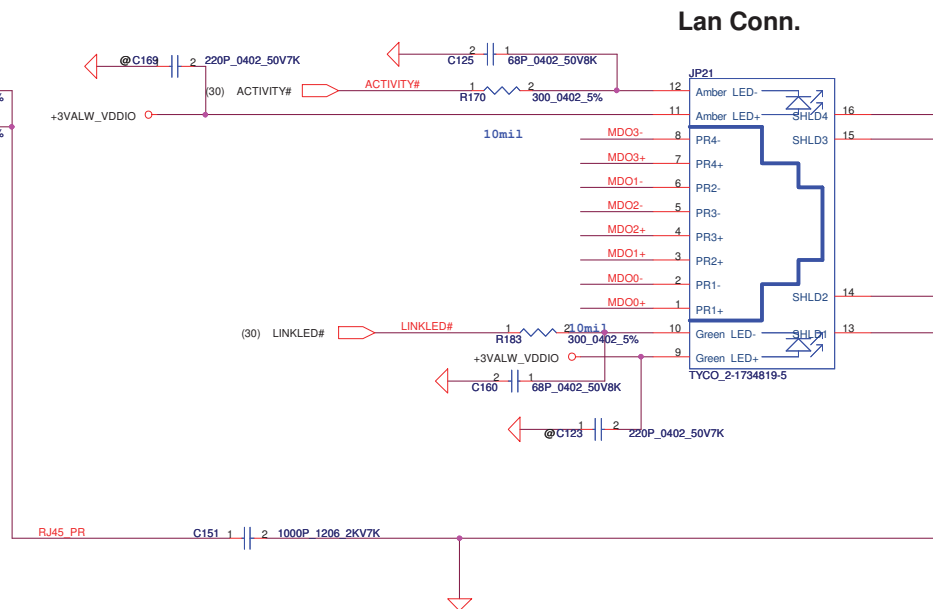
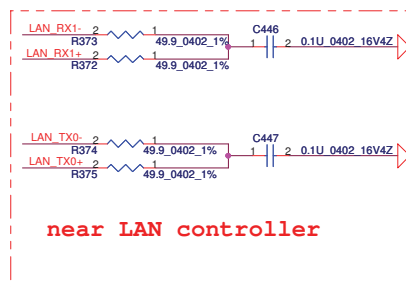


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Compal Electronics, Inc.			
Title			
BCM5787M-GLAN			
Size Custom	Document Number	Rev	
	LA-3861P	0.1	
Date:	Tuesday, August 21, 2007	Sheet	30 of 47



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

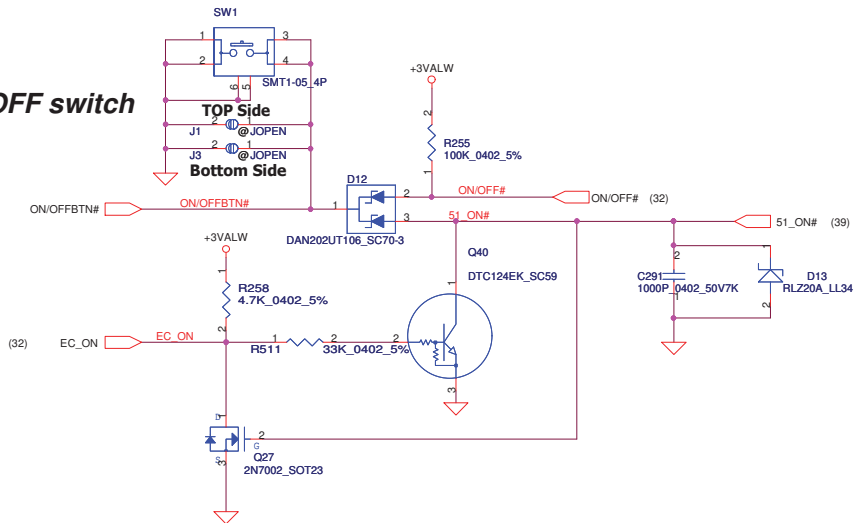


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								LAN CONTROLLER	
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								Custom	0.1
								Date:	
								Monday, August 20, 2007	
								Sheet	
								31	
								of	
								47	

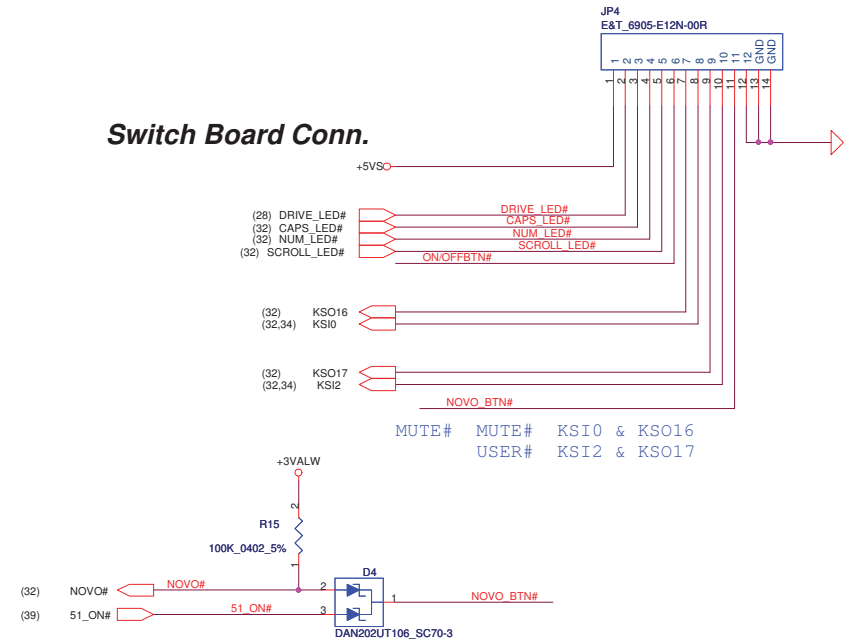


Power Button

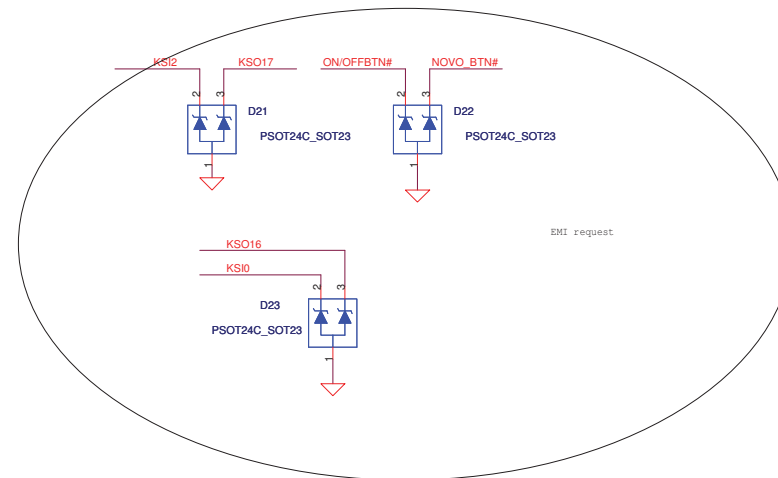
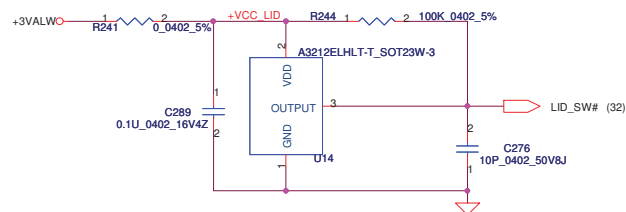
ON/OFF switch



Switch Board Conn.

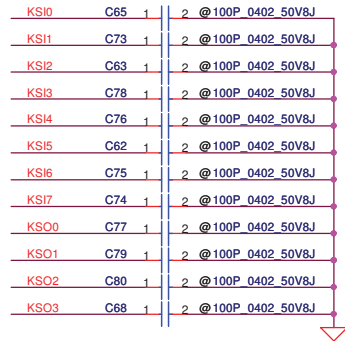
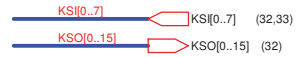


Lid Switch

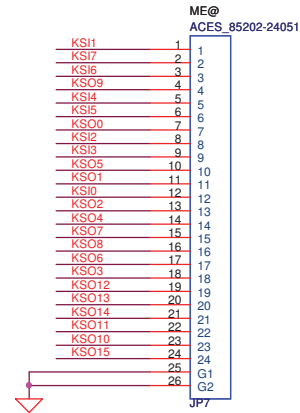


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				B	LA-3861P	0.1
				Date:	Monday, August 20, 2007	Sheet 33 of 47

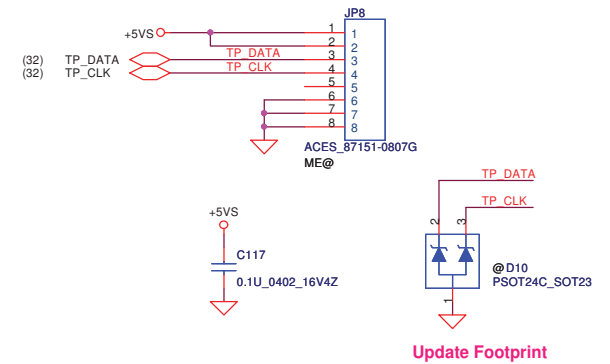
INT_KBD Conn.



For IHL00



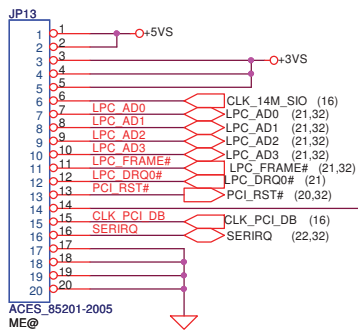
To TP/B Conn.



EC DEBUG PORT

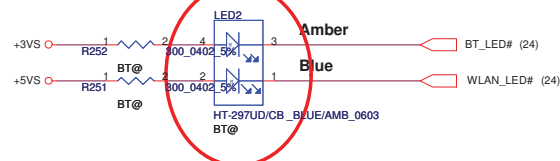
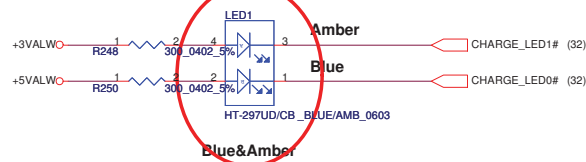
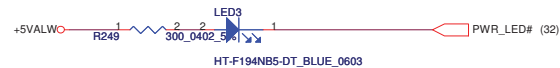


FOR LPC SIO DEBUG PORT



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Size	Document Number	Rev		0.1	
Date:	Monday, August 20, 2007	Sheet	34	of	47

LED

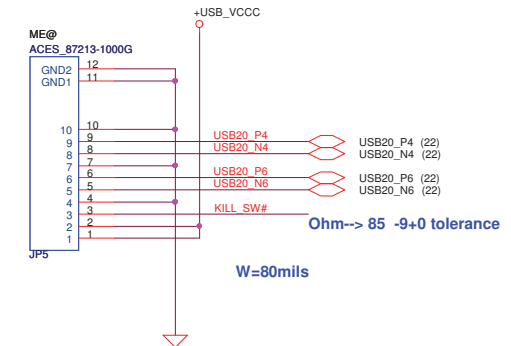
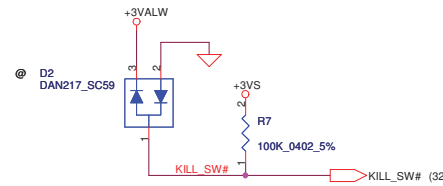


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				Date: Monday, August 20, 2007	Rev 0.1
				Sheet 35 of 47	

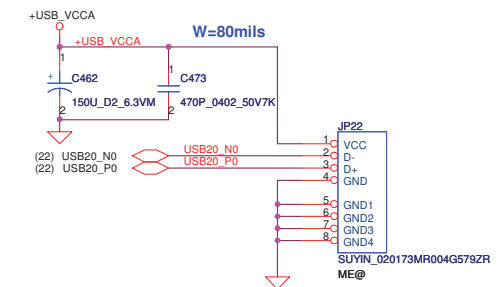
USB Conn.

W=80mils

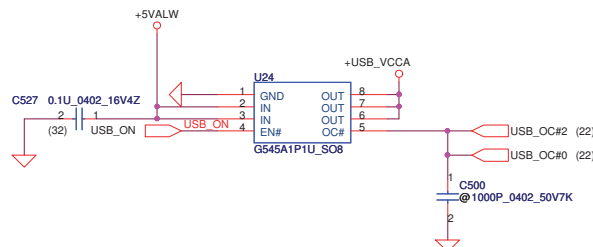
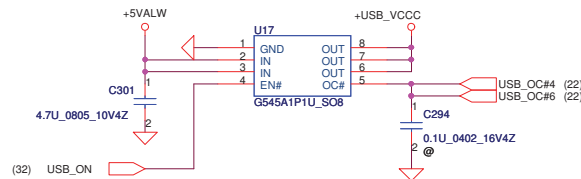
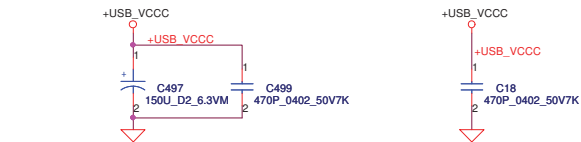
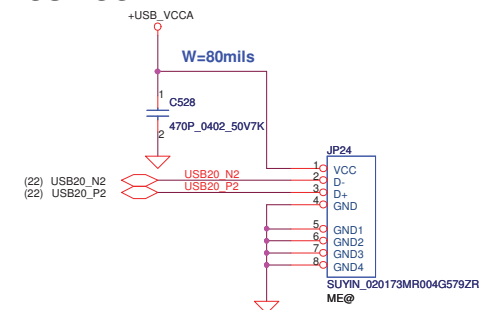
Kill SWITCH



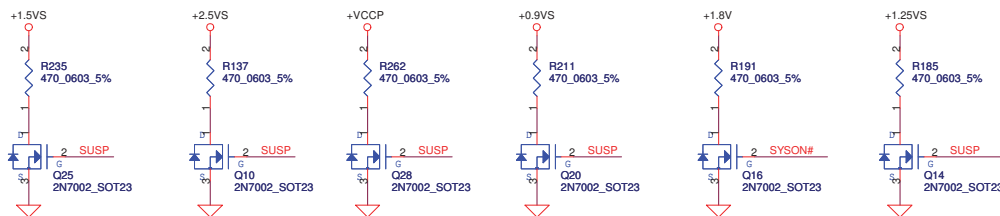
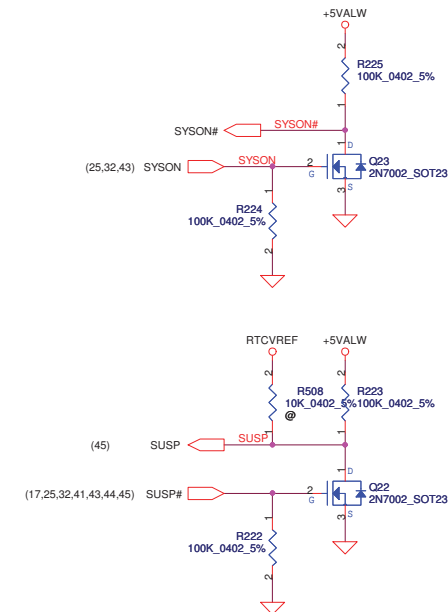
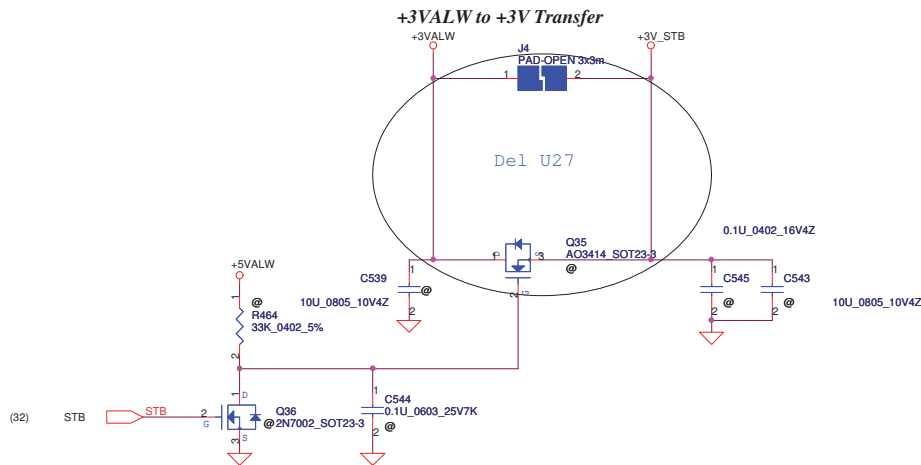
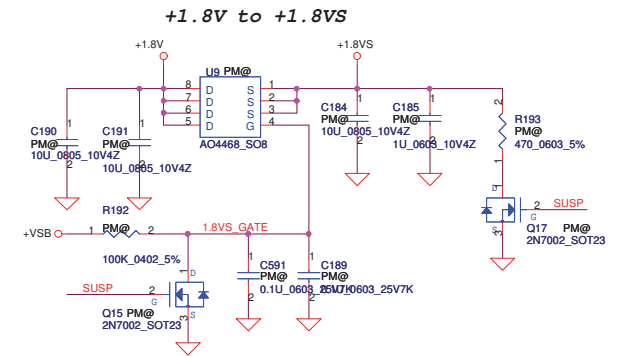
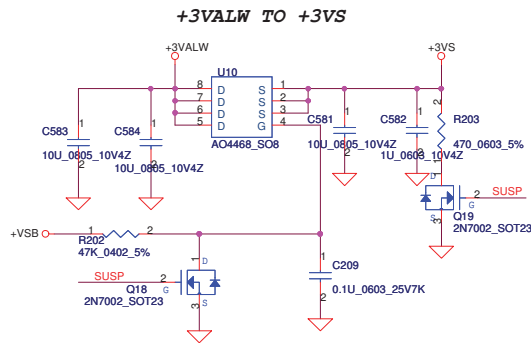
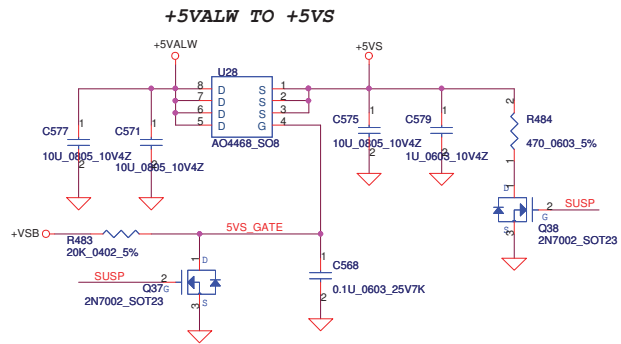
USB CONN. 1



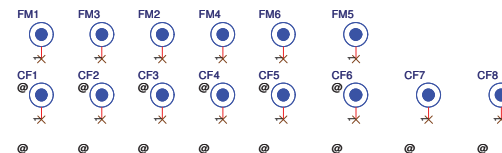
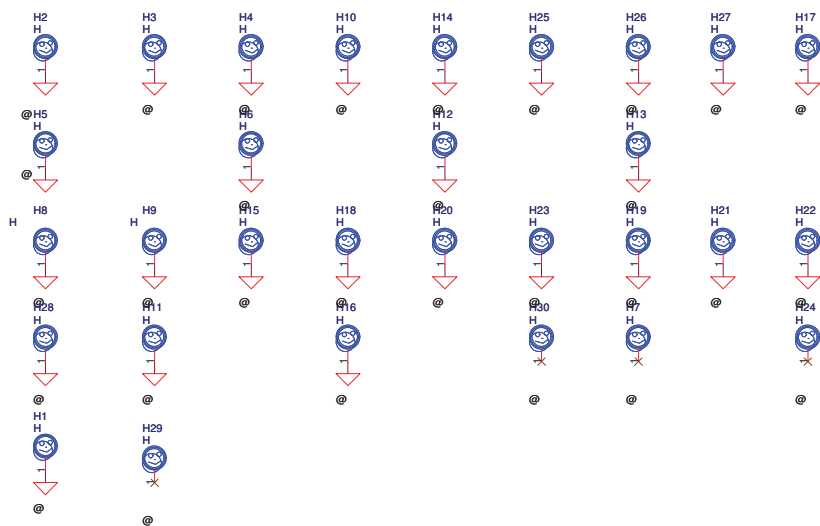
USB CONN. 2



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Issued Date				2006/08/18				Title			
				Deciphered Date				Power OK, Reset and RTC Circuit, TP			
				2007/8/18				Size B			
								Document Number			
								LA-3691P			
								Rev 0.1			
								Date: Monday, August 20, 2007			
								Sheet 36 of 47			



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								DC Interface			
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						Date:	Tuesday, August 21, 2007		Sheet	37	of



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				Date: Monday, August 20, 2007	Rev 0.1
				Sheet 38	of 47

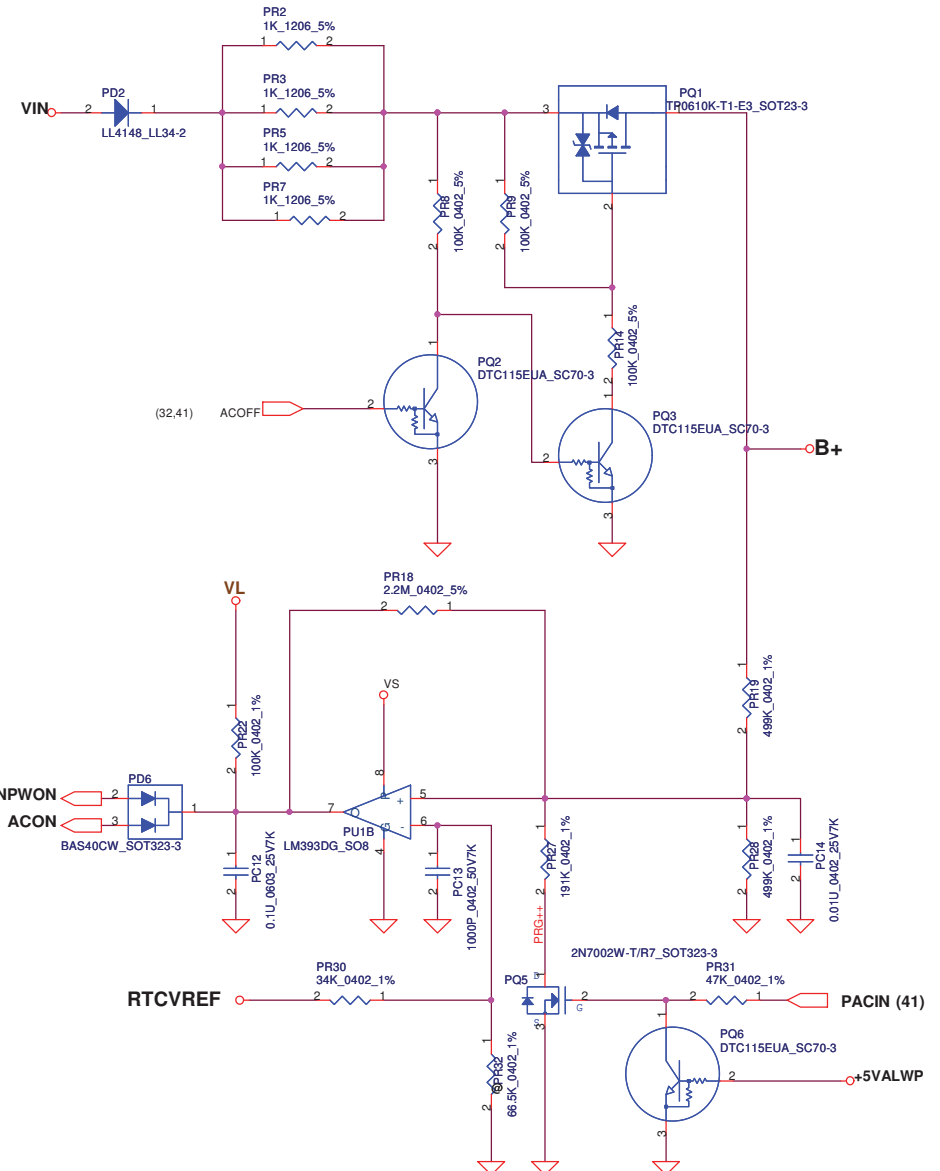
Vin Detector

High	Low
18.764	17.90
17.745	16.9

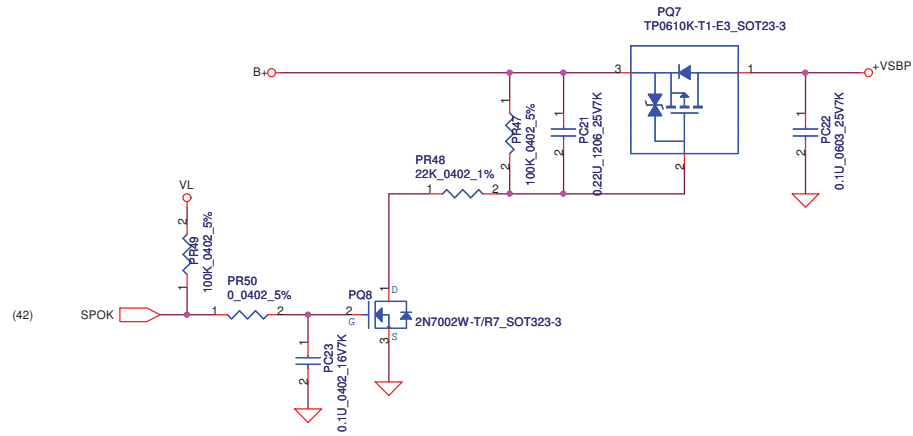
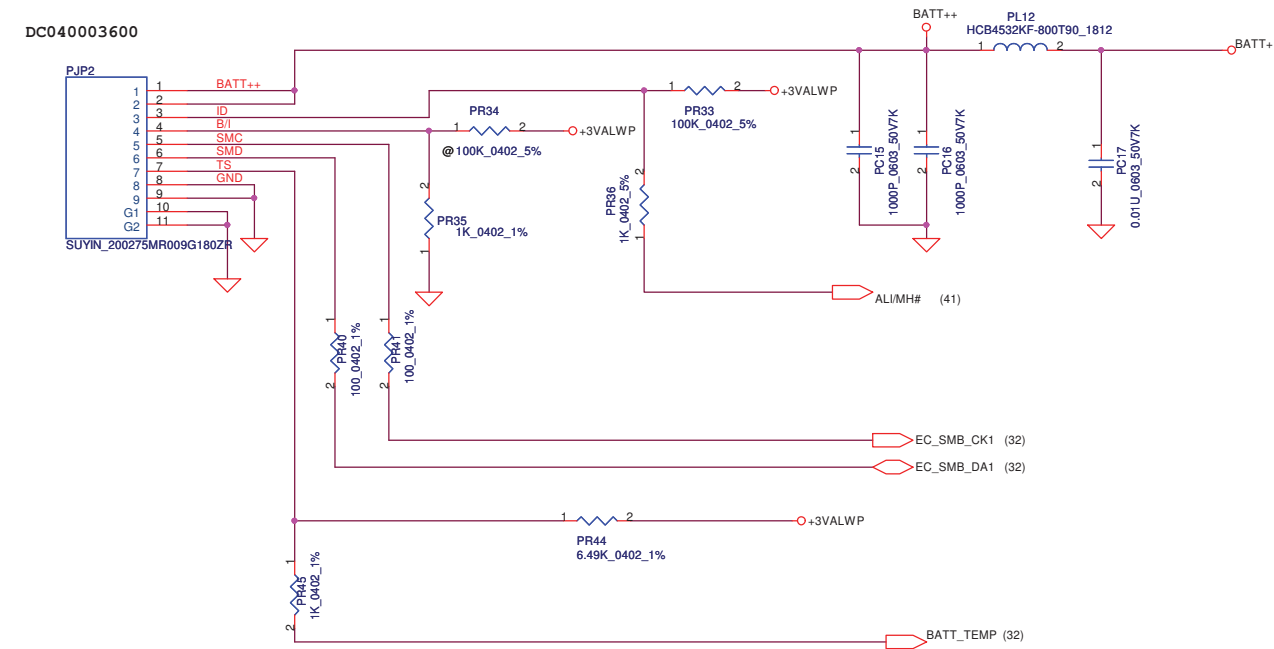
High	18.764	17.901	17.063
Low	17.745	16.9	16.03

Precharge detector		
Min.	typ.	Max.
14.589V	14.84V	15.243V
15.562V	15.97V	16.388V

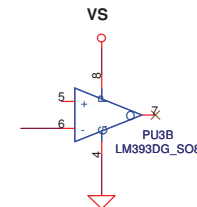
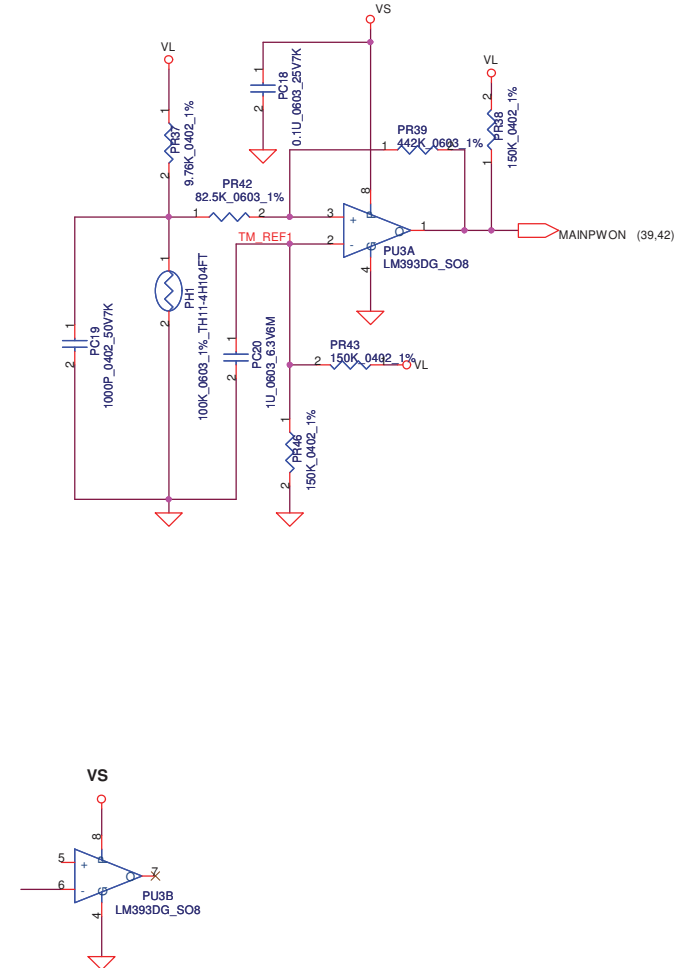
	Precharge detector		
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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					IHL00 LA-3691P	0.3
Date: Monday, August 20, 2007				Sheet 39 of 47		



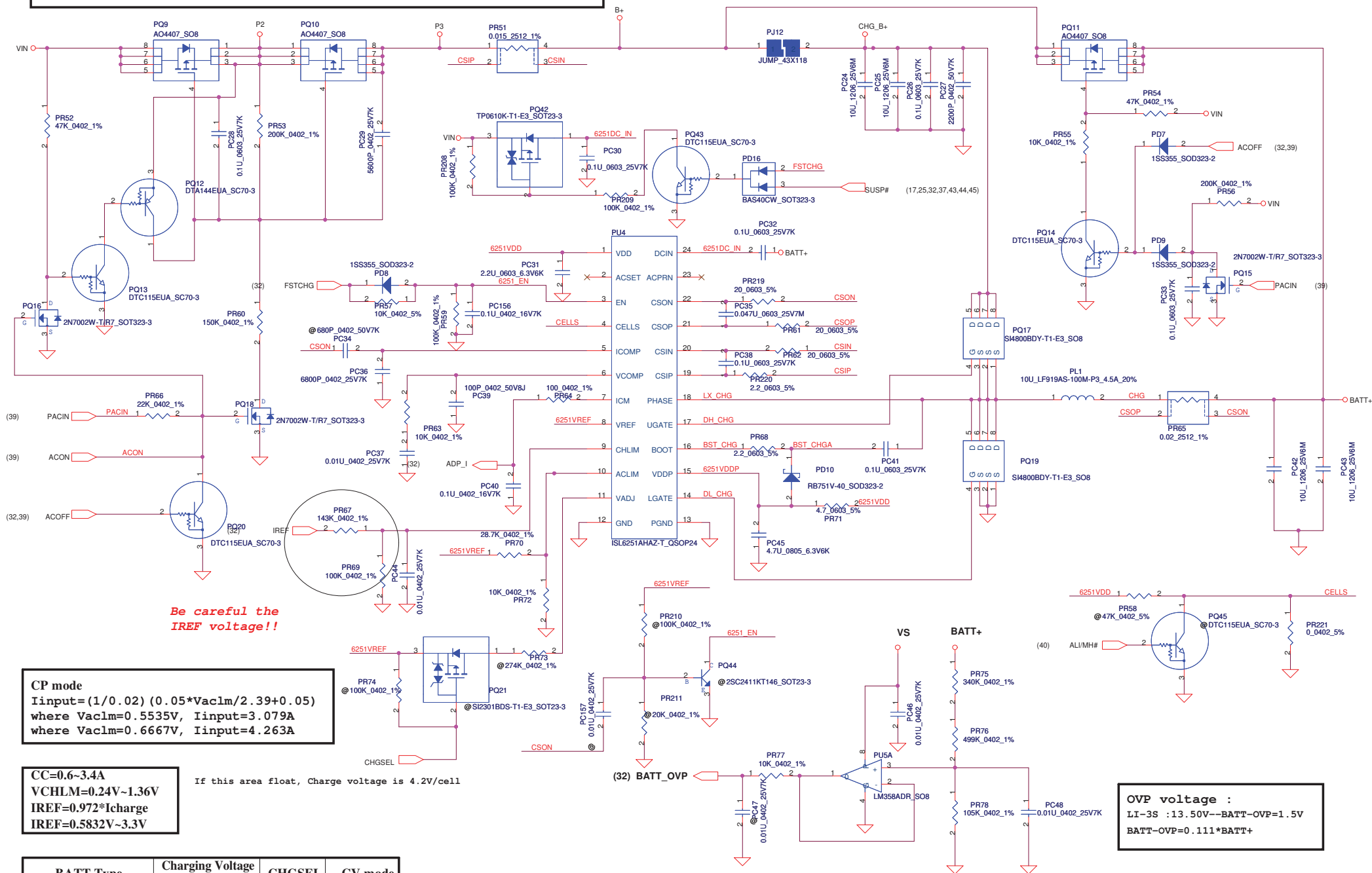
PH1 under CPU bottom side :
CPU thermal protection at 87 degree C
Recovery at 70 degree C



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Size B	Document Number			IHL00 LA-3691P	Rev 0.3
Date:	Monday, August 20, 2007			Sheet 40	of 47

65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR70=39.2K, CP=3.079A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR70=28.7K, CP=4.263A

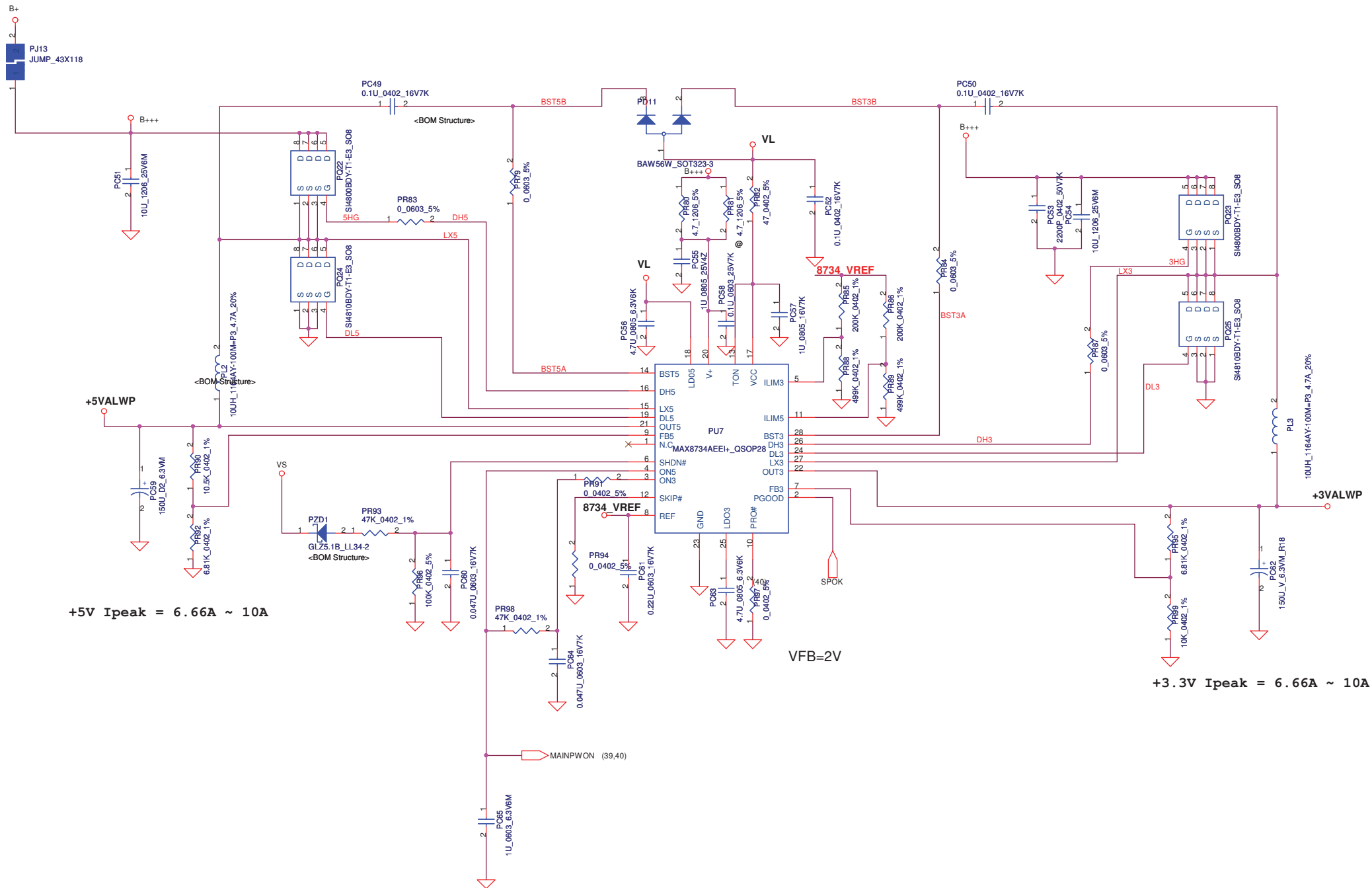
ADP_I = 19.9*Iadapter*Rsense



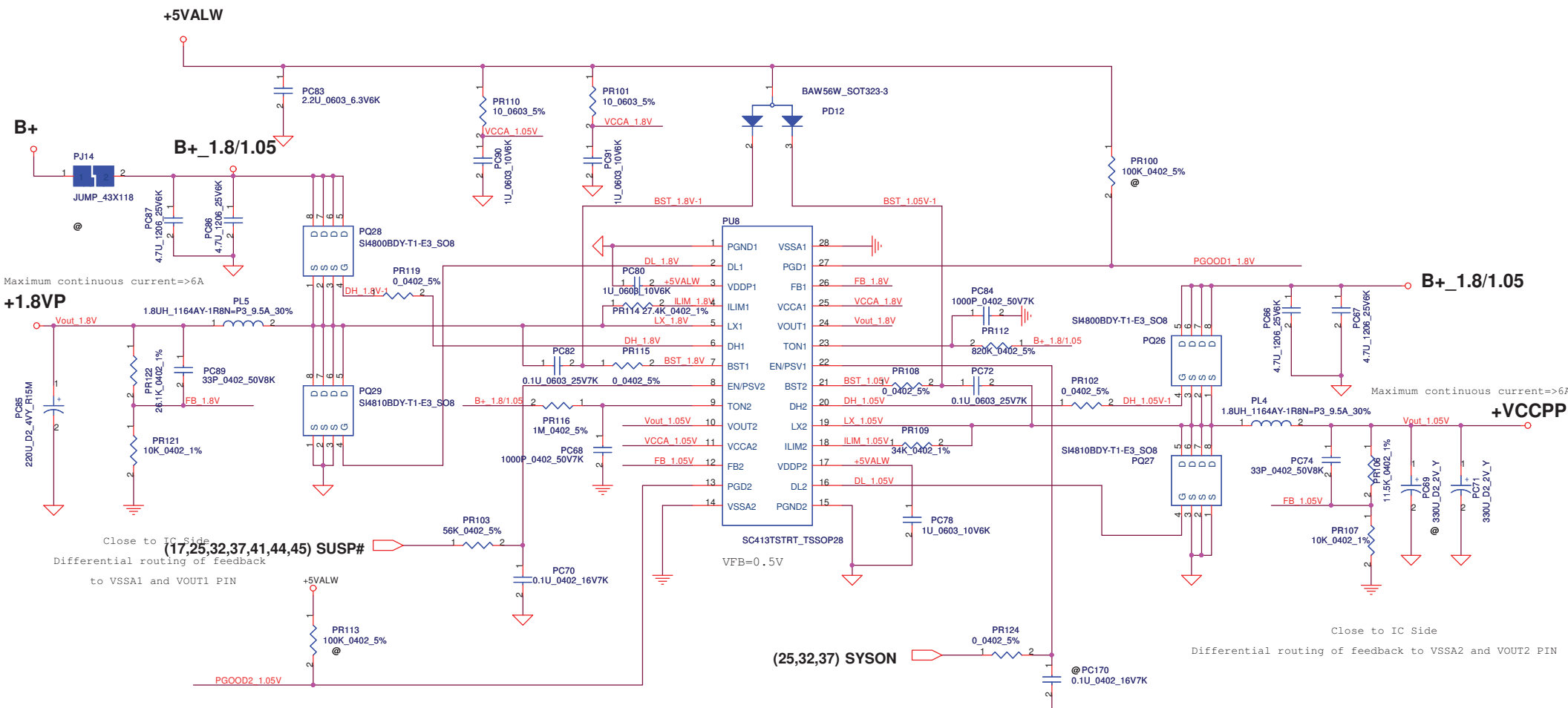
BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V

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CHARGER			
Size	Document Number	IHL00 LA-3691P	
Date:	Monday, August 20, 2007	Sheet	41 of 47



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				Date: Monday, August 20, 2007	Rev 0.3
				Sheet 42	of 47



Maximum continuous current=>6A

Maximum continuous current=>6A

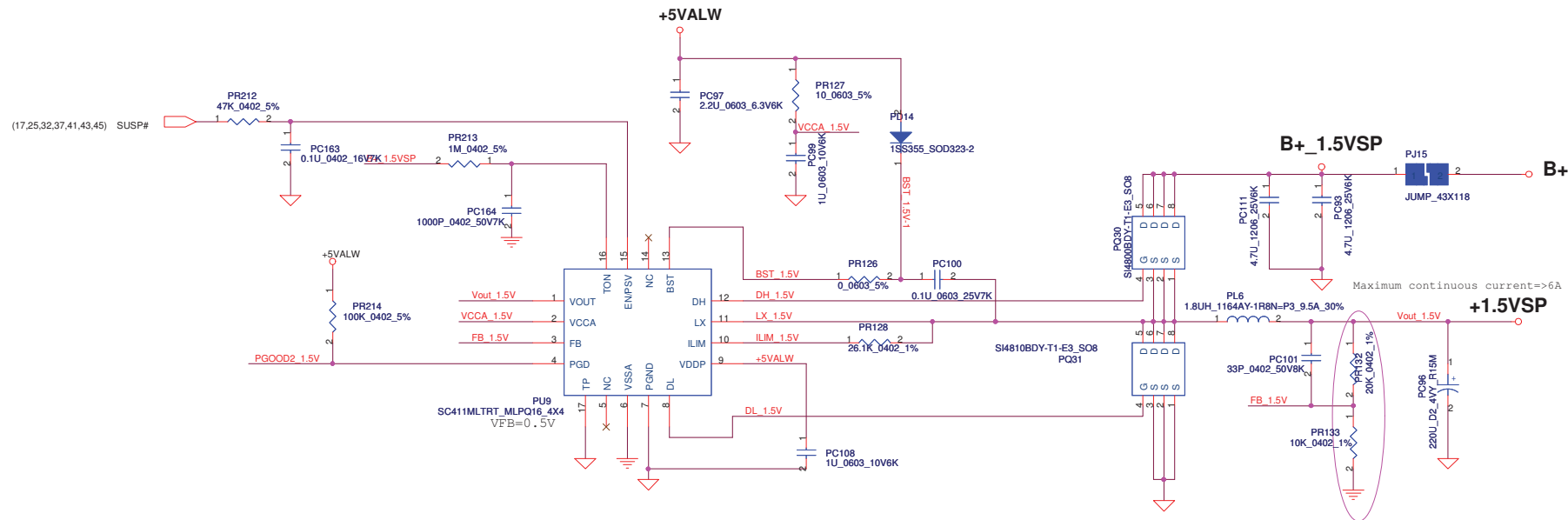
Close to IC Side
Differential routing of feedback
to VSSA1 and VOUT1 PIN

Close to IC Side
Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$
Ipeak=12.17A, Imax=8.519A
 $Ton = (3.3E-12 * (PR121 + 37K) * (Vout / VBat)) + 50ns$
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$
FDS6670AS:Rds(on)=>Typ:9 mOhm
Max:11.5 mOhm
 $Iocp = Ivalley + Iripple / 2$
 $Iripple = (vin - vout) * (Ton / L) = 5.467A, 1/2 Iripple = 2.734A$
 $Ivalleymin = 10E-6 * (PR120 / Rds(ON))max * 1.5$
= 9*10e-6 * (27.4K / 0.0115*1.5) = 14.295A > 11.73*1.2 = 14.076A
 $Ivalleymax = 10E-6 * (PR120 / Rds(ON))typ * 1.2$
= 11*10e-6 * (27.4K / 0.009*1.2) = 27.907A
OCP==>17.029A~30.641A

VFB=0.5V
 $V_o = VFB * (1 + PR129 / PR130) = 1.5V$
Ipeak=5.16A, Imax=3.612A
 $Ton = (3.3E-12 * (PR125 + 37K) * (Vout / VBat)) + 50ns$
 $= 0.3201us$
AO4916 Rds(on)=>Typ:21 mOhm
Max:27 mOhm
Ivalleymin=9*10u* (29.4K / 0.027*1.4) = 7A
 $Ivalleymax = 11E-6 * (29.4K / 0.021*1.1) = 12.833A$
 $Iripple = (vin - vout) * (Ton / L) = 2.546A, 1/2 Iripple = 1.273A$
 $Iocp = Ivalley + Iripple / 2$
OCP==>8.273A~14.106A

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								VCCPP/1.8VP		
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								Custom	IHL00 LA-3691P	0.3
3				2				Date:	Monday, August 20, 2007	Sheet 43 of 47
								1		



Close to IC Side

Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V, Ipeak=14.02A, Imax=9.814A

The current rating of +1.05VSP include +VCC_GFX current.

$V_o = V_{FB} * (1 + PR146 / PR147) = 1.05V$

$Ton = (3.3E-12 * (PR142 + 37K) * (Vout / VBat)) + 50ns = 0.2391\mu s$

$SI4810BDY: Rds(on) \Rightarrow Typ: 9m\Omega$

Max: 11.5 mOhm

$Ivalleymin = 9 * 10E-6 * (PR145 / Rds(ON) max * 1.5)$

$= 9 * 10E-6 * (26.1K / (0.0115 * 1.5)) = 13.617A$

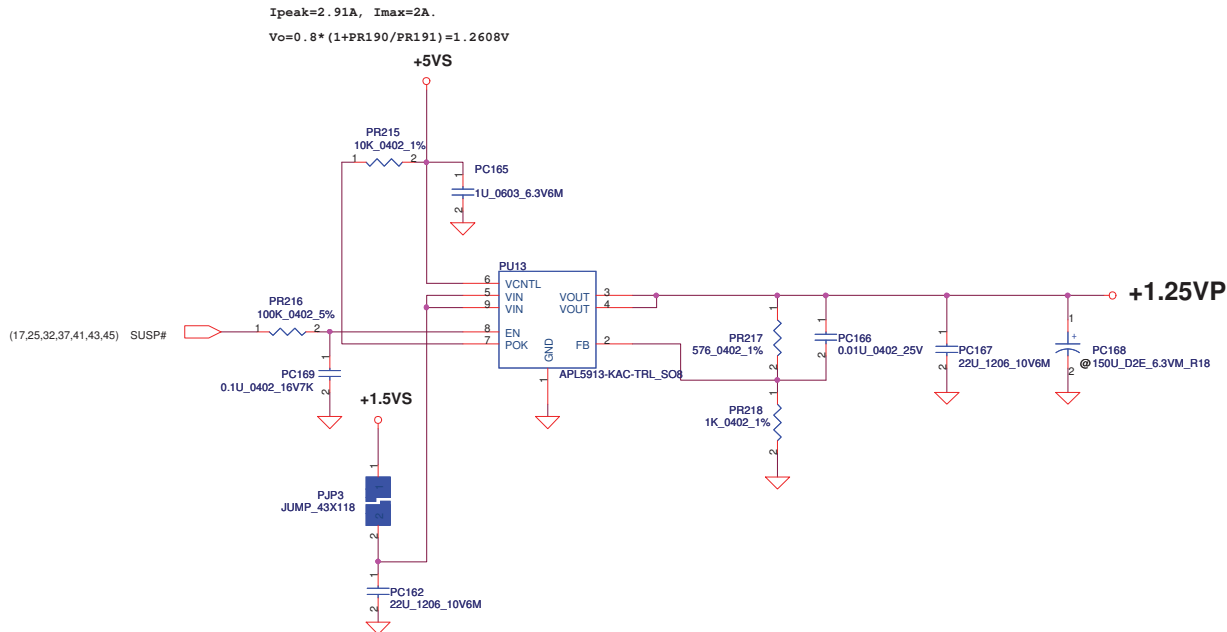
$Ivalleymax = 11 * 10E-6 * (PR145 / Rds(ON) min * 1.2)$

$= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$

$Tripple = (vin - vout) * (Ton / L) = 4.292A, 1/2 Tripple = 2.146A$

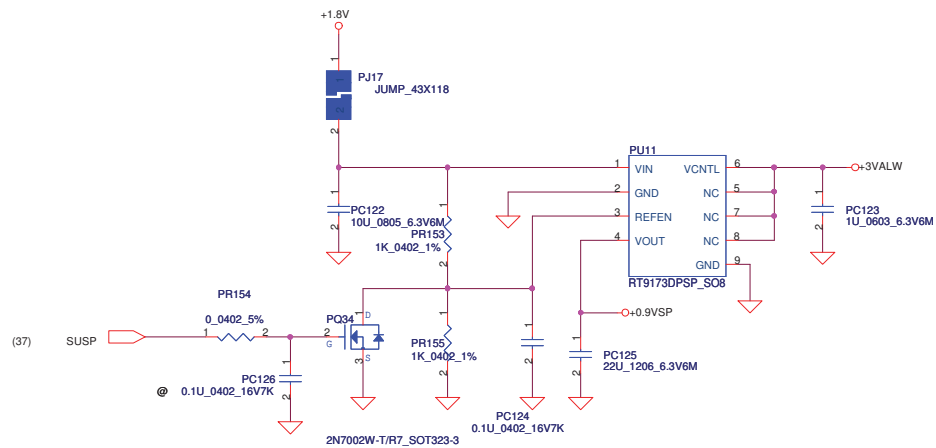
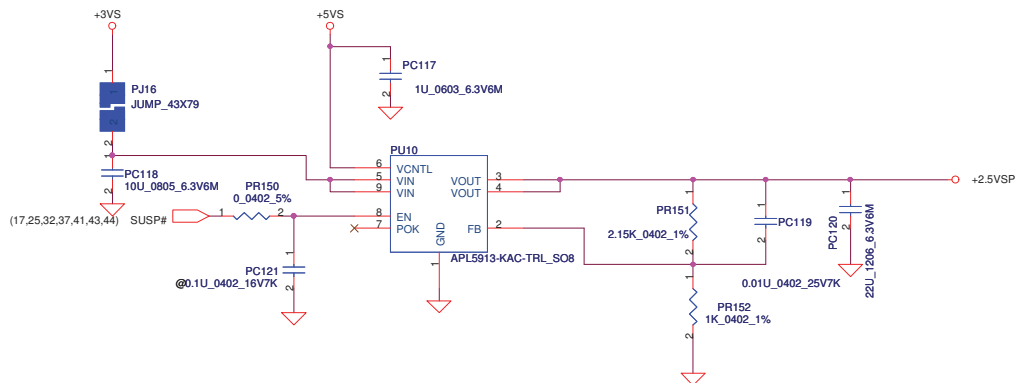
$Iocp = Ivalley + Tripple / 2$

OCP $\Rightarrow 15.763A \sim 22.222A$



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Customer		Rev		Date		Monday, August 20, 2007	
Sheet		44		of		47	

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				+2.5VSP/0.9VSP						
				Size	Document Number			Rev		
				Custom	IHL00 LA-3691P			0.3		
				Date:	Monday, August 20, 2007		Sheet	45	of	47

Version change list (P.I.R. List)

Page 1 of 2
for PWR

[illegible]